ANALYSIS OF CASCADED MULTILEVEL INVERTER INDUCTION MOTOR DRIVES

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ANALYSIS OF CASCADED MULTILEVEL INVERTER INDUCTION MOTOR DRIVES

A Thesis submitted in partial fulfillment of the requirements for the degree of

Master of Technology (Research)
in
Electrical Engineering

By
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CERTIFICATE

This is to certify that the thesis titled **'Analysis of Cascaded Multilevel Inverter Induction Motor Drives'** submitted to the National Institute of Technology, Rourkela by **Mr.Yashobanta Panda, Roll No.60602002** for the award of Master of Technology(Research) in Electrical Engineering, is a bonafide record of research work carried out by him under my supervision and guidance.

The candidate has fulfilled all the prescribed requirements.

The Thesis which is based on candidate's own work, has not submitted elsewhere for a degree/diploma.

In my opinion, the thesis is of standard required for the award of a Master of Technology (Research) degree in Electrical Engineering.

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ACKNOWLEDGEMENTS

I would like to express my sincere appreciation to my supervisor Prof. A. K. Panda, for his guidance, encouragement, and support throughout the course of this thesis work. It was an invaluable learning experience for me to be one of his students. From him I have gained not only extensive knowledge, but also a careful research attitude.

I am very much thankful to Prof. B.D.Subudhi, Head, Department of Electrical Engineering, for his constant support. Also, I am indebted to him for providing me all official and laboratory facilities.

I am grateful to my Master Scrutiny Members, Prof.S.Meher and Prof. K. B. Mohanty for their valuable suggestions and comments during this research period.

I am especially indebted to my colleagues in the power electronics group. First, I would like to specially thank Mr. Y.Suresh, who helped me in implementing my real time experiments. We share our knowledge & experience in the field of power electronics. I would also like to thank the other members of the team, Mr.Swapnajit Patnaik, Mr. Matada Mahesh, Mr. B.K.Debta, for extending their technical and personal support making my stay pleasant and enjoyable.

This section would remain incomplete if I don't thank the lab assistant Mr. Rabindra Nayak and Mr. Chotta Lal Singh, without whom the work would have not progressed.

My heartfelt appreciation goes toward my uncle, Mr. Pratap Kumar Tripathy, my brothers, Jayanta and Jivan and my parents, who were always encouraged me to pursue higher education. With much love, I would like to thank my wife, Susmita, who is always there with her kind and encouraging words. Finally I dedicate this thesis to my son Ayush (Omm).

Y.Panda.

CONTENTS

ABBREVIATIONS

FACTS	**-Flexible AC Transmission Systems**
SVG	**-Static Var Generation**
MLI	**-Multi Level Inverter**
CMC	**-Cascaded Multilevel Converter**
CMI	**-Cascaded Multi-level Inverter**
HBBB	**-H-bridge building block**
PWM	**-Pulse Width Modulation**
SVM	**-Space-Vector Modulation**
CM	**-Common-Mode**
NPC	**-Neutral-Point Clamped**
GTO	**-Gate Turn Off Thyristors**
IGBT	**-Insulated Gate Bipolar Transistor**
ARCP	**-Auxiliary Resonant Commutated Pole**
ZVT	**-Zero-Voltage Transition**
SVM	**-Space Vector Modulation**
THD	**-Total Harmonic Distortion**
SHE	**-Selective Harmonic Elimination**
THD	**-Total Harmonic Distortion**
SVC	**-Space Vector Control**
DTC	**-Direct Torque Control**
UPFC	**-Unified Power-Flow Controller**
VSI	**-Voltage-Source Inverter**

DCI	**-Diode Clamped Inverter**
FCMLI	**-Flying Capacitor Multi Level Inverter**
IGCT	**-Integrate Gate Controlled Thyristor**
HV	**-High Voltage**
LV	**-Low Voltage**
FPGA	**-Field Programmable Gate Array**
EMC	**-Electro Magnetic Compatibility**
IPM	**-Intelligent Power Module**
SPWM	**-Sinusoidal Pulse Width Modulation**
DC	**-Direct Current**
DSP	**-Digital Signal Processing**
EMI	**-Electro Magnetic Interference**
PLD	**-Programmable Logic Device**
CMI	**-Common Mode Interference**
MPC	**-Multiple Point Clamped**
FPGA	**-Field Programmable Gate Arrays**
SPWM	**-Sinusoidal Pulse Width Modulation**

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Abstract

This thesis aims to extend the knowledge about the performance of different cascaded multilevel inverter induction motor drives through harmonic analysis.

Large electric drives and utility applications require advanced power electronics converter to meet the high power demands. As a result, multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations. A multilevel converter not only achieves high power ratings, but also improves the performance of the whole system in terms of harmonics, dv/dt stresses, and stresses in the bearings of a motor. Several multilevel converter topologies have been developed; i) diode clamped, ii) flying capacitors, and iii) cascaded or H-bridge. Referring to the literature reviews, the cascaded multilevel inverter (CMI) with separated DC sources is clearly the most feasible topology for use as a power converter for medium & high power applications due to their modularization and extensibility. The H-bridge inverter eliminates the excessively large number of (i) bulky transformers required by conventional multilevel inverters, (ii) clamping diodes required by multilevel diode-clamped inverters, , and (iii) flying capacitors required by multilevel flying-capacitor inverter.

As a preliminary study the thesis examined and compared the most common multilevel topologies found in the published literature. Starting from the essential requirements, the different approaches to the construction of multilevel inverter are explained and compared. In particular, aspects of total harmonic distortion (THD) and modulation which are required or desirable for multilevel converters are discussed. Sine-triangle carrier modulation is identified as the most promising technique to pursue for both technical and pedagogical reasons.

Since cascaded multilevel inverter is considered to be suitable for medium & high power applications, the thesis examined & compared the harmonic analysis of 3-level, 5-level, & 7-

level cascaded multilevel inverter induction motor drives through analysis, simulation & experiment.

In order to balance the DC capacitor voltages, sine triangle pulse width modulation (SPWM) technique, which is suitable for any number of H-bridge converters, is applied. The applied cascaded PWM algorithm has been practically realized into the field programmable gate arrays (FPGA).

Chapter-1

INTRODUCTION

Research Background

Induction Motor Drives Using Multi-Level Inverter

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INTRODUCTION

1.1 Research Background

Power electronic converters, especially dc/ac PWM inverters have been extending their range of use in industry because they provide reduced energy consumption, better system efficiency, improved quality of product, good maintenance, and so on.

For a medium voltage grid, it is troublesome to connect only one power semiconductor switches directly [1, 2, 3]. As a result, a multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations such as laminators, mills, conveyors, pumps, fans, blowers, compressors, and so on. As a cost effective solution, multilevel converter not only achieves high power ratings, but also enables the use of low power application in renewable energy sources such as photovoltaic, wind, and fuel cells which can be easily interfaced to a multilevel converter system for a high power application.

The most common initial application of multilevel converters has been in traction, both in locomotives and track-side static converters [4]. More recent applications have been for power system converters for VAR compensation and stability enhancement [5], active filtering [6], high-voltage motor drive [3], high-voltage dc transmission [7], and most recently for medium voltage induction motor variable speed drives [8]. Many multilevel converter applications focus on industrial medium-voltage motor drives [3, 9], utility interface for renewable energy systems [10], flexible AC transmission system (FACTS) [11], and traction drive systems [12].

The inverters in such application areas as stated above should be able to handle high voltage and large power. For this reason, two-level high-voltage and large-power inverters have been designed with series connection of switching power devices such as gate-turn-off thyristors (GTOs), integrated gate commutated transistors (IGCTs), and integrated gate bipolar transistors

(IGBTs), because the series connection allows reaching much higher voltages. However, the series connection of switching power devices has big problems [13], namely, non equal distribution of applied device voltage across series-connected devices that may make the applied voltage of individual devices much higher than blocking voltage of the devices during transient and steady-state switching operation of devices.

As alternatives to effectively solve the above-mentioned problems, several circuit topologies of multilevel inverter and converter have been researched and utilized. The output voltage of the multilevel inverter has many levels synthesized from several DC voltage sources. The quality of the output voltage is improved as the number of voltage levels increases, so the quantity of output filters can be decreased.

The concept of multilevel converters has been introduced since 1975. The cascade multilevel inverter was first proposed in 1975 [14]. Separate DC-sourced full-bridge cells are placed in series to synthesize a staircase AC output voltage. The term multilevel began with the three-level converter [15]. Subsequently, several multilevel converter topologies have been developed [16]. In 1981, diode-clamped multilevel inverter also called the Neutral-Point Clamped (NPC) inverter schemes were proposed [17]. In 1992, capacitor-clamped (or flying capacitor) multilevel inverters, [18] and in 1996, cascaded multilevel inverters were proposed [1], [19]. Although the cascade multilevel inverter was invented earlier, its application did not prevail until the mid 1990s. The advantages of cascade multilevel inverters were prominent for motor drives and utility applications. The cascade inverter has drawn great interest due to the great demand of medium-voltage high-power inverters. The cascade inverter is also used in regenerative-type motor drive applications [20, 21]. Recently, some new topologies of multilevel inverters have emerged. This includes generalized multilevel inverters [22], mixed multilevel

inverters [23], hybrid multilevel inverters [24, 25] and soft-switched multilevel inverters [26]. These multilevel inverters can extend rated inverter voltage and power by increasing the number of voltage levels. They can also increase equivalent switching frequency without the increase of actual switching frequency, thus reducing ripple component of inverter output voltage and electromagnetic interference effects.

A multilevel converter can be implemented in many different ways. The simplest techniques involve the parallel or series connection of conventional converters to form the multilevel waveforms [27]. More complex structures effectively insert converters within converters [28]. The voltage or current rating of the multilevel converter becomes a multiple of the individual switches, and so the power rating of the converter can exceed the limit imposed by the individual switching devices.

The elementary concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple dc voltage sources. The commutation of the power switches aggregate these multiple dc sources in order to achieve high voltage at the output; however, the rated voltage of the power semiconductor switches depends only upon the rating of the dc voltage sources to which they are connected.

A multilevel converter has several advantages over a conventional two-level converter that uses high switching frequency pulse width modulation (PWM). The attractive features of a multilevel converter can be briefly summarized as follows.

1. Staircase waveform quality: Multilevel converters not only can generate the output voltages with very low distortion, but also can reduce the dv/dt stresses; therefore electromagnetic compatibility (EMC) problems can be reduced.
2. Common-mode (CM) voltage: Multilevel converters produce smaller CM voltage; therefore, the stress in the bearings of a motor connected to a multilevel motor drive can be reduced. Furthermore, CM voltage can be eliminated by using advanced modulation strategies such as that proposed in [29].
3. Input current: Multilevel converters can draw input current with low distortion.
4. Switching frequency: Multilevel converters can operate at both fundamental switching frequency and high switching frequency PWM. It should be noted that lower switching frequency usually means lower switching loss and higher efficiency.

Multilevel converters do have some disadvantages. One particular disadvantage is the greater number of power semiconductor switches needed. Although lower voltage rated switches can be utilized in a multilevel converter, each switch requires a related gate drive circuit. This may cause the overall system to be more expensive and complex.

Abundant modulation techniques and control paradigms have been developed for multilevel converters such as sinusoidal pulse width modulation (SPWM), selective harmonic elimination (SHE-PWM), space vector modulation (SVM), and others. In this thesis sinusoidal pulse width modulation (SPWM) is used.

1.2 Induction motor drives using multi-level inverter.

Many current and future designs will incorporate the use of induction motors as the primary source for traction in electric vehicles. Designs for heavy duty trucks and many military combat vehicles that have large electric drives will require advanced power electronic inverters

to meet the high power demands (>250 kw). Development of electric drive trains for these large vehicles will result in increased fuel efficiency, lower emissions, and likely better vehicle performance (acceleration and braking). Multilevel inverters are uniquely suited for these applications because of the high VA ratings possible with these inverters.

The first railway-traction-drive application of a three-level PWM converter and inverter system is the class 1822 dual-voltage locomotive of Austrian Railways (OBB) [30]. Three-level inverter schemes were proposed by *Nabae et al.* in 1981 [31]. The three-level configuration was used initially because of the high-voltage DC-operation requirement. The available 4.5kV gate-turnoff thyristor (GTO) devices are not suitable for a two-level scheme operating directly off 3kV DC catenaries. Here the three-level configuration was used to achieve higher power and lower harmonics at both the input and output of the traction drive.

The multilevel voltage source inverters unique structure allows them to reach high voltages and power levels without the use of transformers [32]. They are specially suited to high voltage vehicle drives where low output voltage total harmonic distortion (THD) and electromagnetic interference (EMI) are needed. The general function of the multilevel inverter is to synthesize a desired voltage from several levels of dc voltages. For this reason, multilevel inverters can easily provide the high power required of a large EV or HEV drive.

As the number of levels increases, the synthesized output waveform has more steps, which produces a staircase wave that approaches the desired waveform. Also, as more steps are added to the waveform, the harmonic distortion of the output wave decreases, approaching zero as the number of levels increases. As the number of levels increases, the voltage that can be spanned by connecting devices in series also increases. The structure of the multilevel inverter is such that no voltage sharing problems are encountered by the active devices [33]. Using

multilevel inverters as drives for automotive electric motors is a much different application than for the utility applications for which they were originally developed [1, 34, 35].

Three, five, and seven level rectifier-inverter drive systems which have used some form of multilevel PWM as a means to control the switching of the rectifier and inverter sections have been investigated in the literature [36-37]. Multilevel PWM has lower dv/dt than that experienced in some two- level PWM drives because switching is between several smaller voltage levels.

First, the silicon-controlled rectifier (SCR) or thyristor was developed, which made the voltage-regulation requirement for DC traction motors much easier. Then the gate-turnoff thyristor was developed, which made the three-phase induction-motor inverter drive become a standard. Now the insulated-gate bipolar transistor (IGBT) is taking over from the GTO and is expected to consolidate the supremacy of the inverter drive and further improve its performance.

The development of high-voltage, high current IGBTs may well change the outcome of the debate regarding two-level and three-level schemes. The arguments in favor of the two-level scheme are that it is cheaper, simpler and therefore more reliable. However, the three-level & higher level schemes are not much more expensive, it has better performance electrically and environmentally and the reliability will be improved with the development of high-voltage and current intelligent power modules (IPM) which have integral gate-drive and self-protection functions.

1.3 Why Cascaded H-bridge multilevel inverter?

Cascaded H-Bridge (CHB) configuration has recently become very popular in high-power AC supplies and adjustable-speed drive applications. A cascade multilevel inverter consists of a series of H-bridge (single-phase full bridge) inverter units in each of its three

phases. Each H-bridge unit has its own dc source, which for an induction motor would be a battery unit, fuel cell or solar cell. Each SDC (separate D.C. source) is associated with a single-phase full-bridge inverter. The ac terminal voltages of different level inverters are connected in series. Through different combinations of the four switches, S1-S4, each converter level can generate three different voltage outputs, *+Vdc*, *-Vdc* and zero. The AC outputs of different full-bridge converters in the same phase are connected in series such that the synthesized voltage waveform is the sum of the individual converter outputs. Note that the number of output-phase voltage levels is defined in a different way from those of the two previous converters (i.e. diode clamped and flying capacitor). In this topology, the number of output-phase voltage levels is defined by m= 2N+1, where N is the number of DC sources. A seven-level cascaded converter, for example, consists of three DC sources and three full bridge converters. Minimum harmonic distortion can be obtained by controlling the conducting angles at different converter levels. Each H- bridge unit generates a quasi-square waveform by phase shifting its positive and negative phase legs' switching timings. Each switching device always conducts for 180° (or half cycle) regardless of the pulse width of the quasi-square wave. This switching method makes all of the switching devices current stress equal. In the motoring mode, power flows from the batteries through the cascade inverters to the motor. In the charging mode, the cascade converters act as rectifiers, and power flows from the charger (ac source) to the batteries. The cascade converters can also act as rectifiers to help recover the kinetic energy of the vehicle if regenerative braking is used. The cascade inverter can also be used in parallel HEV configurations. This new converter can avoid extra clamping diodes or voltage balancing capacitors.

The combination of the 180° conducting method and the pattern-swapping scheme make the cascade inverter's voltage and current stresses the same and battery voltage balanced.

Identical H-bridge inverter units can be utilized, thus improving modularity and manufacturability and greatly reducing production costs. Battery-fed cascade inverter prototype driving an induction motor at 50% and 80% rated speed both the voltage and current are almost sinusoidal. Electromagnetic interference (EMI) and common mode voltage are also much less than what would result from a PWM inverter because of the inherently low dv/dt and sinusoidal voltage output.

The main advantages of using the cascade inverter in an induction motor include:

(1) It makes induction motor more accessible/safer and open wiring possible for most of an induction motor power system.

(2) Traditional 230 V or 460 V motors can be used, thus higher efficiency is expected as compared to low voltage motors.

(3) No EMI problem or common-mode voltage/current problem exists.

(4) Low voltage switching devices can be used.

(5) No charge unbalance problem exists in both charge mode and drive mode.

Cascade inverters are ideal for an induction motor that has many separate dc sources (batteries) available for the individual H-bridges, these inverters are not an option for series hybrid induction motors because cascade inverters cannot be easily connected back-to-back. For series-configured induction motors where an onboard combustion engine generates ac power via an alternator or generator, a multilevel back-to-back diode clamped converter drive can best interface with the source of ac power and yet still easily meet the high power and/or high voltage requirements of the induction motor.

Induction motors generally have an ac voltage source from an alternator or combustion-engine generator. A rectifier converts this ac voltage to dc for the electric energy storage devices on

board – batteries or ultra capacitors. An inverter converts the dc voltage to variable voltage variable frequency ac in order to drive the main induction motor.

The multilevel converter can act as an inverter in drive mode when energy is being sent to the motor that drives the wheels and as a rectifier during regenerative braking or during charge mode when the vehicle is plugged into an external ac source.

The reduction in dv/dt can prevent motor windings and bearings from failure. The staircase output voltage waveform approaches a sine wave, thus having no common-mode voltage and no voltage surge to the motor windings.

A cascaded multilevel inverter is discussed to eliminate the excessively large number of

(1) bulky transformers required by conventional multi pulse inverters,

(2) clamping diodes required by multilevel diode-clamped inverters, and

(3) flying capacitors required by multilevel flying-capacitor inverters.

Also, it has the following features:

1. It is much more suitable to high-voltage, high-power applications than the conventional inverters.

2. It switches each device only once per line cycle and generates a multistep staircase voltage waveform approaching a pure sinusoidal output voltage by increasing the number of levels.

3. Since the inverter structure itself consists of a cascade connection of many single-phase, full-bridge inverter (FBI) units and each bridge is fed with a separate DC source, it does not require voltage balance (sharing) circuits or voltage matching of the switching devices.

4. Packaging layout is much easier because of the simplicity of structure and lower component count.

5. Soft-switching can be used in this structure to avoid bulky and lossy resistor-capacitor-diode snubbers.

These advantages are our motivation to work on the harmonic analysis of cascaded three-level, five-level & seven-level induction motor drives.

1.4 Dissertation Outline

This dissertation intends to analyze the performance and effectiveness of the CMC-based Induction motor drives and it is divided into the following five chapters.

Chapter 1 discusses merits & demerits of cascaded multilevel inverter & discusses briefly the application of multilevel inverter in industries.

Chapter 2 presents the topological issues in multi-level inverter. The literature written about multilevel VSI's are discussed. All published VSI topologies are categorized based on their structures and are compared based on their performances.

Chapter 3 discuses different aspects of modulation techniques which are required or desirable for multilevel converters. Sine-triangle carrier modulation is identified as the most promising technique to pursue for both technical and pedagogical reasons. Natural and uniform sampled sine-triangle modulation are examined and contrasted in detail.

Chapter 4 presents the Induction Motor drives with cascaded multilevel inverters. Simulation and experimental results are presented for 3-level, 5-level and 7-level inverter induction motor drives.

Chapter 5 draws conclusion for this dissertation and proposes future work.

Chapter 2

MULTILEVEL INVERTER STRUCTURES

Diode-Clamped Multilevel Inverter

Flying Capacitor Multilevel Inverter

Cascaded Multilevel Inverter

Mixed-Level Hybrid Multilevel Inverter

Soft Switching Multilevel Inverters

Multilevel Inverter structures

A voltage level of three is considered to be the smallest number in multilevel converter topologies. Due to the bi-directional switches, the multilevel VSC can work in both rectifier and inverter modes. This is why most of the time it is referred to as a converter instead of an inverter in this dissertation. A multilevel converter can switch either its input or output nodes (or both) between multiple (more than two) levels of voltage or current. As the number of levels reaches infinity, the output THD approaches zero. The number of the achievable voltage levels, however, is limited by voltage-imbalance problems, voltage clamping requirements, circuit layout and packaging constraints complexity of the controller, and, of course, capital and maintenance costs.

Three different major multilevel converter structures have been applied in industrial applications: cascaded H-bridges converter with separate dc sources, diode clamped, and flying capacitors. The multilevel inverter structures are the main focus of discussion in this chapter; however, the illustrated structures can be implemented for rectifying operation as well. Although each type of multilevel converters share the advantages of multilevel voltage source inverters, they may be suitable for specific application due to their structures and drawbacks. Operation and structure of some important type of multilevel converters are discussed in the following sections.

In a multilevel VSI, the dc-link voltage V_{dc} is obtained from any equipment which can yield stable dc source. Series connected capacitors constitute energy tank for the inverter providing some nodes to which multilevel inverter can be connected. Primarily, the series connected capacitors will be assumed to be any voltage sources of the same value. Each capacitor voltage V_c is given by $V_c=V_{dc}/(n-1)$, where n denotes the number of level.

Fig. 2.1 shows a schematic diagram of one phase leg of inverters with different number of levels, for which the action of the power semiconductors is represented by an ideal switch with several positions. A two-level inverter generates an output voltage with two values (levels) with respect to the negative terminal of the capacitor, while the three-level inverter generates three voltages, and so on.

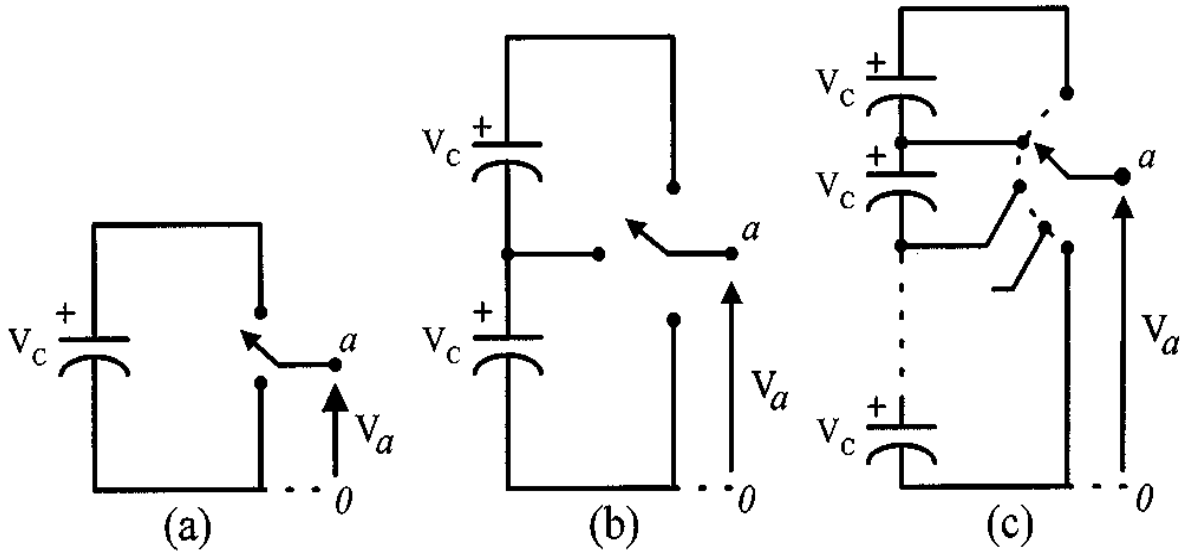

Fig. 2.1 One phase leg of an inverter with (a) two levels, (b) three levels, and (c) n levels.

2.1 Diode-Clamped Multilevel Inverter

The most commonly used multilevel topology is the diode clamped inverter, in which the diode is used as the clamping device to clamp the dc bus voltage so as to achieve steps in the output voltage. The neutral point converter proposed by Nabae, Takahashi, and Akagi in 1981 was essentially a three-level diode-clamped inverter [15]. A three-level diode clamped inverter consists of two pairs of switches and two diodes. Each switch pairs works in complimentary mode and the diodes used to provide access to mid-point voltage. In a three-level inverter each of the three phases of the inverter shares a common dc bus, which has been subdivided by two

capacitors into three levels. The DC bus voltage is split into three voltage levels by using two series connections of DC capacitors,C1 and C2. The voltage stress across each switching device is limited to V_{dc} through the clamping diodes Dc1 and Dc2. It is assumed that the total dc link voltage is V_{dc} and mid point is regulated at half of the dc link voltage, the voltage across each capacitor is $V_{dc}/2$ ($Vc1=Vc2=V_{dc}/2$). In a three level diode clamped inverter, there are three different possible switching states which apply the stair case voltage on output voltage relating to DC link capacitor voltage rate. For a three-level inverter, a set of two switches is on at any given time and in a five-level inverter, a set of four switches is on at any given time and so on. Fig-2.2 shows the circuit for a diode clamped inverter for a three-level and a five-level inverter. Switching states of the three level inverter are summarized in table-1.

Table-2.1. Switching states in one leg of the three-level diode clamped inverter

Switch Status	State	Pole Voltage
S_1=ON,S_2=ON $S_{1'}$=OFF,$S_{2'}$=OFF	S=+ve	V_{ao}=Vdc/2
S_1=OFF,S_2=ON $S_{1'}$=ON,$S_{2'}$=OFF	S=0	V_{ao}=0
S_1=OFF,S_2=OFF $S_{1'}$=ON,$S_{2'}$=ON	S=-ve	V_{ao}=-Vdc/2

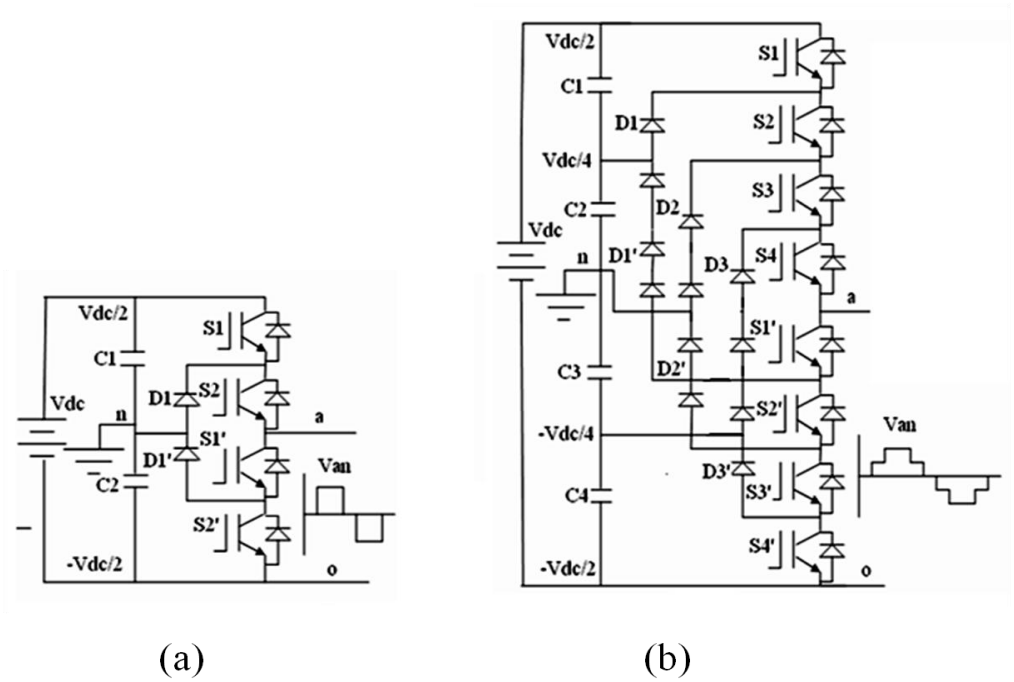

Fig 2.2: Topology of the diode-clamped inverter (a) three-level inverter, (b) five -level inverter

Fig 2.3 shows the phase voltage and line voltage of the three-level inverter in the balanced condition. The line voltage V_{ab} consists of a phase-leg *a* voltage and a phase-leg *b* voltage. The resulting line voltage is a 5-level staircase waveform for three-level inverter and 9-level staircase waveform for a five-level inverter. This means that an N-level diode-clamped inverter has an N-level output phase voltage and a (2N-1)-level output line voltage. In general the voltage across each capacitor for an N level diode clamped inverter at steady state is V_{dc}/ (N-1). Although each active switching device is required to block only a voltage level of V_{dc}, the clamping diodes require different ratings for reverse voltage blocking.

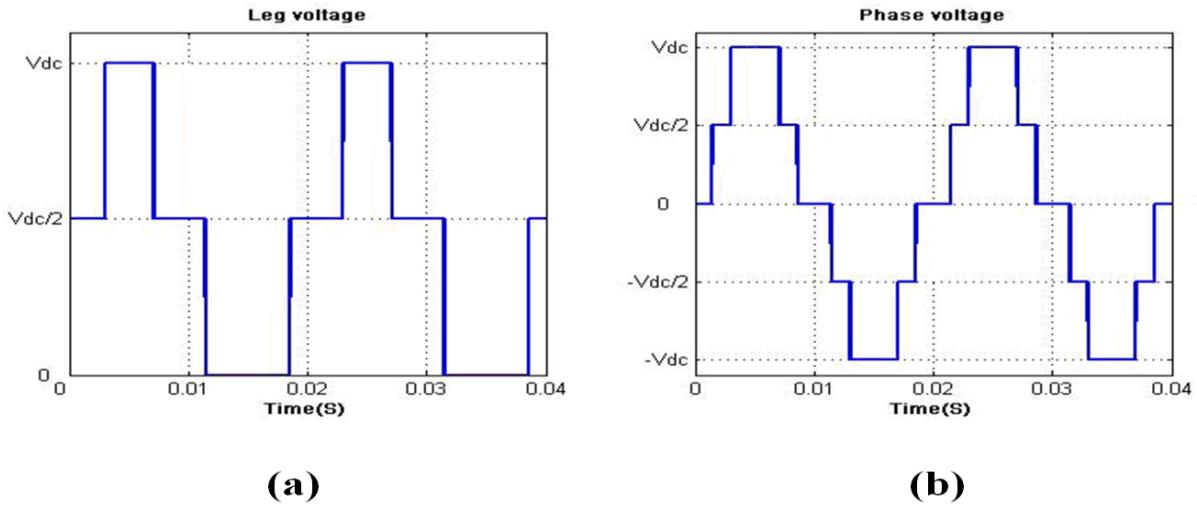

Fig: 2.3 .Output voltage in three-level diode- clamped inverter (a) leg voltage

(b) output phase voltage

In general for an N level diode clamped inverter, for each leg 2(N-1) switching devices, (N-1) * (N-2) clamping diodes and (N-1) dc link capacitors are required. By increasing the number of voltage levels the quality of the output voltage is improved and the voltage waveform becomes closer to sinusoidal waveform. However, capacitor voltage balancing will be the critical issue in high level inverters. When N is sufficiently high, the number of diodes and the number of switching devices will increase and make the system impracticable to implement. If the inverter runs under pulse width modulation (PWM), the diode reverse recovery of these clamping diodes becomes the major design challenge.

Though the structure is more complicated than the two-level inverter, the operation is straightforward.

2.1.1 Operation of DCMLI.

Fig 2.2(a) shows a three-level diode-clamped converter in which the dc bus consists of two capacitors, C_1, C_2. For dc-bus voltage V_{dc}, the voltage across each capacitor is $V_{dc}/2$ and each device voltage stress will be limited to one capacitor voltage level Vdc/2 through clamping

diodes. To explain how the staircase voltage is synthesized, the neutral point n is considered as the output phase voltage reference point. There are three switch combinations to synthesize three-level voltages across a and n.

1) Voltage level $V_{an} = V_{dc}/2$, turn on the switches $S_1$and$S_{2.}$

2) Voltage level $V_{an} = 0$, turn on the switches S_2 and $S_{1'}$.

3) Voltage level $V_{an} = - V_{dc}/2$ turn on the switches $S_{1'}$,S_2'.

Fig. 2.2(b) shows a five-level diode-clamped converter in which the dc bus consists of four capacitors, C_1, C_2, C_3, and C_4. For dc-bus voltage V_{dc}, the voltage across each capacitor is $V_{dc}/4$ and each device voltage stress will be limited to one capacitor voltage level Vdc/4 through clamping diodes.

Switching states of the five level inverter are summarized in table-2.2.

Table-2.2. Switching states in one leg of the five-level diode clamped inverter

Voltage Vao	Switch state							
	S1	S2	S3	S4	S1’	S2’	S3’	S4’
Vao=Vdc	1	1	1	1	0	0	0	0
Vao=Vdc/2	0	1	1	1	1	0	0	0
Vao=0	0	0	1	1	1	1	0	0
Vao=-Vdc/2	0	0	0	1	1	1	1	0
Vao=-Vdc	0	0	0	0	1	1	1	1

To explain how the staircase voltage is synthesized, the neutral point n is considered as the output phase voltage reference point. There are five switch combinations to synthesize five level voltages across a and n.

1) Voltage level $V_{an} = V_{dc}$; turn on all upper switches S_1 , S_2 , S_3 and S_4.

2) Voltage level $V_{an}= V_{dc}/2$, turn on the switches S_2, S_3, S_4 and $S_{1'}$.

3) Voltage level $V_{an}= 0$, turn on the switches S_3, S_4, $S_{1'}$ and $S_{2'}$.

4) Voltage level $V_{an}= - V_{dc}/2$ turn on the switches S_4, $S_{1'}$, S_2', $S_{3'}$.

5) Voltage level $V_{an}= - V_{dc}$; turn on all lower switches $S_{1'}$, $S_{2'}$, $S_{3'}$ and $S_{4'}$.

Four complementary switch pairs exist in each phase. The complementary switch pair is defined such that turning on one of the switches will exclude the other from being turned on. In this example, the four complementary pairs are ($S_1 - S_1'$), ($S_2 - S_2'$), ($S_3 - S_3'$), and ($S_4 - S_4'$).

Although each active switching device is only required to block a voltage level of V_{dc}/ (m-1), the clamping diodes must have different voltage ratings for reverse voltage blocking. Using D_1' of Fig. 2.2(b) as an example, when lower devices S_2'- S_4', are turned on, D_1'needs to block three capacitor voltages, or $3V_{dc}/4$, and D_1 needs to block $V_{dc}/4$. Similarly, D_2 and D_2' need to block $2V_{dc}/4$, and D_3 needs to block $3V_{dc}/4$. Assuming that each blocking diode voltage rating is the same as the active device voltage rating, the number of diodes required for each phase will be (*m*-1)*(*m*-2). This number represents a quadratic increase in *m*.

There are some complementary switches and in a practical implementation, some dead time is inserted between the gating signals and their complements meaning that both switches in a complementary pair may be switched off for a small amount of time during a transition. However, for the discussion herein, the dead time will be ignored.

2.1.2 Features of Diode clamped MLI

1) High-Voltage Rating Required for Blocking Diodes:

Although each active switching device is only required to block a voltage level of Vdc/(m - l), the clamping diodes need to have different voltage ratings for reverse voltage blocking.

Using $D_{1'}$ of Fig. 2 (5-level diode clamped inverter) as an example, when all lower devices, S_1'-S_4' are turned on, D_1' needs to block three capacitor voltages, or 3Vdc/4. Similarly, D_2 and D_2' need to block 2Vdc/4, and D_3 needs to block 3Vdc/4. Assuming that each blocking diode voltage rating is the same as the active device voltage rating, the number of diodes required for each phase will be *(m* - 1) x (m - 2). This number represents a quadratic increase in *m*. When *m* is sufficiently high, the number of diodes required will make the system impractical to implement.

2) *Unequal Device Rating*,

In figure-2 it can be seen that switch S_1 conducts only during *Vao* = Vdc, while switch S_4 conducts over the entire cycle except during *Vao* = 0. Such an unequal conduction duty requires different current ratings for switching devices. When the inverter design is to use the average duty for all devices, the outer switches may be oversized, and the inner switches may be undersized. If the design is to suit the worst case, then each phase will have 2 x *(m* - 2) outer devices oversized. In comparison with the traditional transformer coupling multipulse converters using six-step operation for each converter, such unequal conduction duty is indeed an advantageous feature because the six-step operation needs maximum duty in each device and circulating currents between converters through transformers.

3) Capacitor Voltage Unbalance:

In most applications, a power converter needs to transfer real power from ac to dc (rectifier operation) or dc to ac (inverter operation). When operating at unity power factor, the charging time for rectifier operation (or discharging time for inverter operation) for each capacitor is different. Such a capacitor charging profile repeats every half cycle, and the result is unbalanced capacitor voltages between different levels. The voltage unbalance problem in a multilevel converter can be solved by several approaches, such as replacing capacitors by a

controlled constant dc voltage source such as pulse-width modulation (PWM) voltage regulators or batteries. The use of a controlled dc voltage will result in system complexity and cost penalties. With the high power nature of utility power systems, the converter switching frequency must be kept to a minimum to avoid switching losses and electromagnetic interference (EMI) problems. When operating at zero power factor, however, the capacitor voltages can be balanced by equal charge and discharge in one-half cycle. This indicates that the converter can transfer pure reactive power without the voltage unbalance problem.

2.1.3 Advantages and Disadvantages of DCMLI.

Advantages:

1. All of the phases share a common dc bus, which minimizes the capacitance requirements of the converter. For this reason, a back-to-back topology is not only possible but also practical for uses such as a high-voltage back-to-back inter-connection or an adjustable speed drive.
2. The capacitors can be pre-charged as a group.
3. Efficiency is high for fundamental frequency switching.
4. When the number of levels is high enough, harmonic content will be low enough to avoid the need for filters

Disadvantages:

1. Real power flow is difficult for a single inverter because the intermediate dc levels will tend to overcharge or discharge without precise monitoring and control.
2. The number of clamping diodes required is quadratically related to the number of levels [1], which can be cumbersome for units with a high number of levels.

2.1.4 Conclusion

The diode-clamped inverter provides multiple voltage levels through connection of the phases to a series of capacitors. The concept can be extended to any number of levels by increasing the number of capacitors. Early descriptions of this topology were limited to three-levels where two capacitors are connected across the dc bus resulting in one additional level. The additional level was the neutral point of the dc bus, so the terminology neutral point clamped (NPC) inverter was introduced. However, with an even number of voltage levels, the neutral point is not accessible, and the term multiple point clamped (MPC) is sometimes applied. Due to capacitor voltage balancing issues, the diode-clamped inverter implementation has been limited to three level. Because of industrial developments over the past several years, the three level inverter is now used extensively in industrial application.

2.2 Flying Capacitor Structure.

The capacitor clamped inverter alternatively known as flying capacitor was proposed by *Meynard* and *Foch* in 1992 [18]. The structure of this inverter is similar to that of the diode-clamped inverter except that instead of using clamping diodes, the inverter uses capacitors in their place. The flying capacitor involves series connection of capacitor clamped switching cells. This topology has a ladder structure of dc side capacitors, where the voltage on each capacitor differs from that of the next capacitor. The voltage increment between two adjacent capacitor legs gives the size of the voltage steps in the output waveform. Figure 2.4 shows the three-level and five-level capacitor clamped inverters respectively.

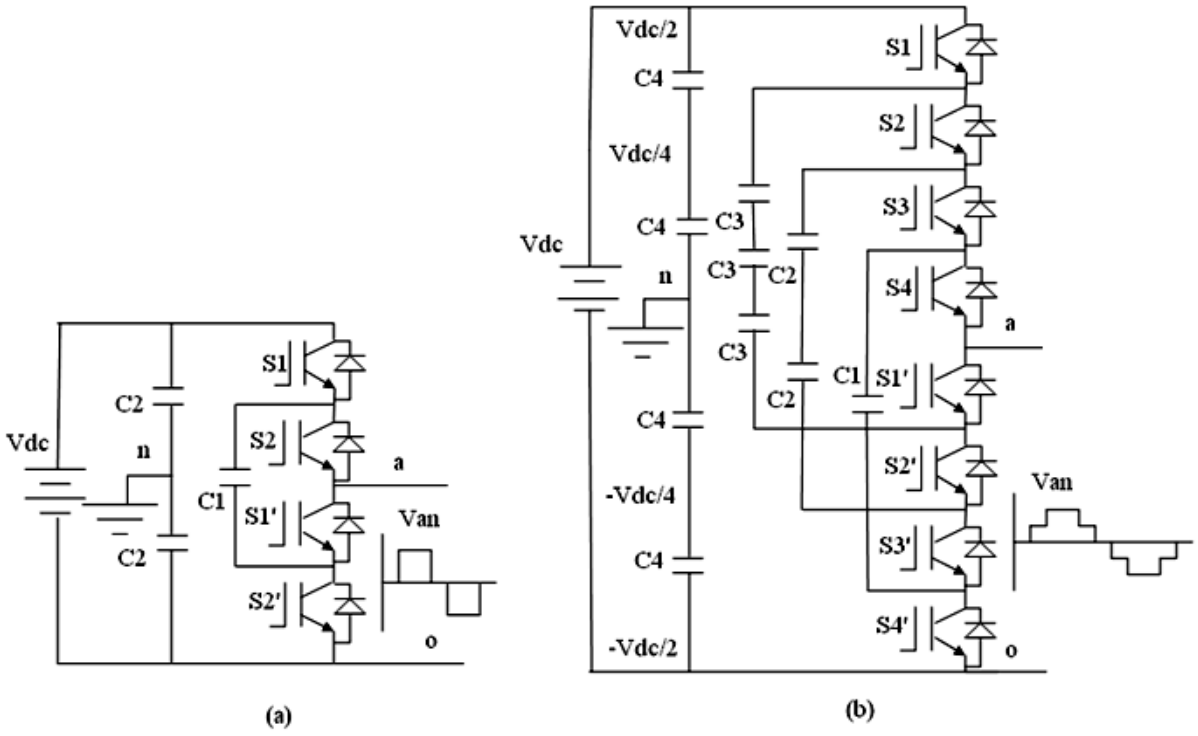

Fig.2.4 Capacitor-clamped multilevel inverter circuit topologies,
(a) 3-level inverter (b) 5- level inverter.

2.2.1. Operation of FCMLI.

In the operation of flying capacitor multi-level inverter, each phase node (a, b, or c) can be connected to any node in the capacitor bank (V_3, V_2, V_1). Connection of the a-phase to positive node V_3 occurs when S_1 and S_2 are turned on and to the neutral point voltage when S_2 and $S_{1'}$ are turned on. The negative node V_1 is connected when $S_{1'}$ and $S_{2'}$are turned on. The clamped capacitor C_1 is charged when S_1 and $S_{1'}$ are turned on and is discharged when S_2 and $S_{2'}$ are turned on. The charge of the capacitor can be balanced by proper selection of the zero states. In comparison to the three-level diode-clamped inverter, an extra switching state is possible. In particular, there are two transistor states, which make up the level V_3. Considering the direction

of the a-phase flying capacitor current I_a for the redundant states, a decision can be made to charge or discharge the capacitor and therefore, the capacitor voltage can be regulated to its desired value by switching within the phase. As with the three-level flying capacitor inverter, the highest and lowest switching states do not change the charge of the capacitors. The two intermediate voltage levels contain enough redundant states so that both capacitors can be regulated to their ideal voltages.

Similar to the diode clamped inverter, the capacitor clamping requires a large number of bulk capacitors to clamp the voltage. Provided that the voltage rating of each capacitor used is the same as that of the main power switch, an N level converter will require a total of (N-1) * (N-2) / 2 clamping capacitors per phase in addition to the (N-1) main dc bus capacitors.

Unlike the diode-clamped inverter, the flying-capacitor inverter does not require all of the switches that are on (conducting) in a consecutive series. Moreover, the flying-capacitor inverter has phase redundancies, whereas the diode-clamped inverter has only line-line redundancies [1, 3]. These redundancies allow a choice of charging/discharging specific capacitors and can be incorporated in the control system for balancing the voltages across the various levels.

The voltage synthesis in a five-level capacitor-clamped converter has more flexibility than a diode-clamped converter. Using Fig. 2.4(b) as the example, the voltage of the five-level phase-leg 'a' output with respect to the neutral point n (i.e.V_{an}), can be synthesized by the following switch combinations.

1) Voltage level $V_{an} = V_{dc}/2$, turn on all upper switches S_1 - S_4 .

2) Voltage level $V_{an} = V_{dc}/4$, there are three combinations.

a) Turn on switches S_1 , S_2 , S_3 and S_1'.($V_{an} = V_{dc}/2$ of upper C_4's - $V_{dc}/4$ of C_1's).

b) Turn on switches S_2 , S_3 , S_4 and S_4'.($V_{an} = 3V_{dc}/4$ of upper C_3's - $V_{dc}/2$ of C_4's).

c) Turn on switches S_1 , S_3 , S_4 and S_3'. (V_{an}= V_{dc}/2 of upper C_4's - 3V_{dc}/4 or C_3's + V_{dc}/2 of upper C_2').

3) Voltage level V_{an}= 0, turn on upper switches S_3 , S_4 , and lower switch S_1', S_2'.

4) Voltage level V_{an}= -V_{dc}/4, turn on upper switch S_1 and lower switches S_1', $S_{2'}$and S_3'.

5) Voltage level V_{an}= -V_{dc}/2, turn on all lower switches S_1', $S_{2'}$, $S_{3'}$ and S_4'.

2.2.2 Features of FCMLI

The major problem in this inverter is the requirement of a large number of storage capacitors. Provided that the voltage rating of each capacitor used is the same as that of the main power switch, an m-level converter will require a total of *(m* - 1) x *(m* - 2)/2 auxiliary capacitors per phase leg in addition to (m - 1) main dc bus capacitors. With the assumption that all capacitors have the same voltage rating, an m-level diode-clamp inverter only requires *(m* - 1) capacitors.

In order to balance the capacitor charge and discharge, one may employ two or more switch combinations for middle voltage levels (i.e., 3Vdc/4. Vdc/2, and Vdc/4) in one or several fundamental cycles. Thus, by proper selection of switch combinations, the flying-capacitor multilevel converter may be used in real power conversions. However, when it involves real power conversions, the selection of a switch combination becomes very complicated, and the switching frequency needs to be higher than the fundamental frequency. In summary, advantages and disadvantages of a flying capacitor multilevel voltage source converter are as follows.

2.2.3 Advantages and Disadvantages of (FCMLI).

Advantages

Compared to the diode-clamped inverter, this topology has several unique and attractive features as described below:

i) Added clamping diodes are not needed.

ii) It has switching redundancy within the phase, which can be used to balance the flying capacitors so that only one dc source is needed.

iii) The required number of voltage levels can be achieved without the use of the transformer. This assists in reducing the cost of the converter and again reduces power loss.

iv) Unlike the diode clamped structure where the series string of capacitors share the same voltage, in the capacitor-clamped voltage source converter the capacitors within a phase leg are charged to different voltage levels.

v) Real and reactive power flow can be controlled.

vi) The large number of capacitors enables the inverter to ride through short duration outages and deep voltage sags.

Disadvantages

i) Converter initialization i.e., before the converter can be modulated by any modulation scheme the capacitors must be set up with the required voltage level as the initial charge. This complicates the modulation process and becomes a hindrance to the operation of the converter.

ii) Control is complicated to track the voltage levels for all of the capacitors.

iii) Precharging all of the capacitors to the same voltage level and startup are complex.

iv) Switching utilization and efficiency are poor for real power transmission.

v) Since the capacitors have large fractions of the dc bus voltage across them, rating of the capacitors are a design challenge.

vi) The large numbers of capacitors are both more expensive and bulky than clamping diodes in multilevel diode-clamped converters.

vii) Packaging is also more difficult in inverters with a high number of levels.

2.3 Cascaded multilevel inverter

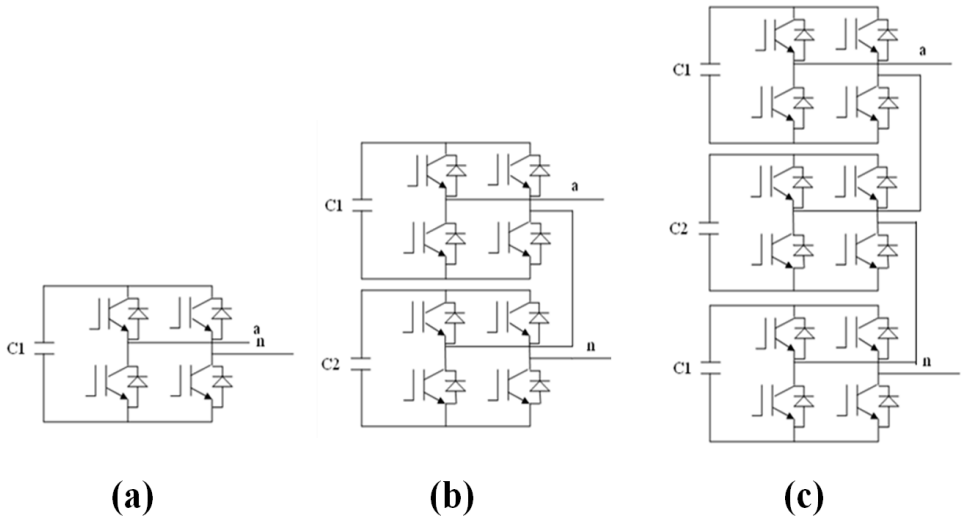

Fig 2.5: Single phase structures of Cascaded inverter (a) 3-level, (b)5-level, (c) 7-level

One more alternative for a multilevel inverter is the cascaded multilevel inverter or series H-bridge inverter. The series H-bridge inverter appeared in 1975[14]. Cascaded multilevel inverter was not fully realized until two researchers, Lai and Peng. They patented it and presented its various advantages in 1997. Since then, the CMI has been utilized in a wide range of applications. With its modularity and flexibility, the CMI shows superiority in high-power applications, especially shunt and series connected FACTS controllers. The CMI synthesizes its output nearly sinusoidal voltage waveforms by combining many isolated voltage levels. By adding more H-bridge converters, the amount of Var can simply increased without redesign the power stage, and build-in redundancy against individual H-bridge converter failure can be realized. A series of single-phase full bridges makes up a phase for the inverter. A three-phase CMI topology is essentially composed of three identical phase legs of the series-chain of H-bridge converters, which can possibly generate different output voltage waveforms and offers the potential for AC system phase-balancing. This feature is impossible in other VSC topologies

utilizing a common DC link. Since this topology consists of series power conversion cells, the voltage and power level may be easily scaled. The dc link supply for each full bridge converter is provided separately, and this is typically achieved using diode rectifiers fed from isolated secondary windings of a three-phase transformer. Phase-shifted transformers can supply the cells in medium-voltage systems in order to provide high power quality at the utility connection.

2.3.1 Operation of CMLI.

The converter topology is based on the series connection of single-phase inverters with separate dc sources. Fig. 2.5 shows the power circuit for one phase leg of a three-level , five-level and seven-level cascaded inverter. The resulting phase voltage is synthesized by the addition of the voltages generated by the different cells. In a 3-level cascaded inverter each single-phase full-bridge inverter generates three voltages at the output: $+V_{dc}$, 0, $-V_{dc}$ (zero, positive dc voltage, and negative dc voltage). This is made possible by connecting the capacitors sequentially to the ac side via the power switches. The resulting output ac voltage swings from $-V_{dc}$ to $+V_{dc}$ with three levels, $-2V_{dc}$ to $+2V_{dc}$ with five-level and $-3V_{dc}$ to $+3V_{dc}$ with seven-level inverter. The staircase waveform is nearly sinusoidal, even without filtering.

For a three-phase system, the output voltage of the three cascaded converters can be connected in either wye (Y) or delta (Δ) configurations. For example, a wye-configured 7-level converter using a CMC with separated capacitors is illustrated in the fig. 2.6.

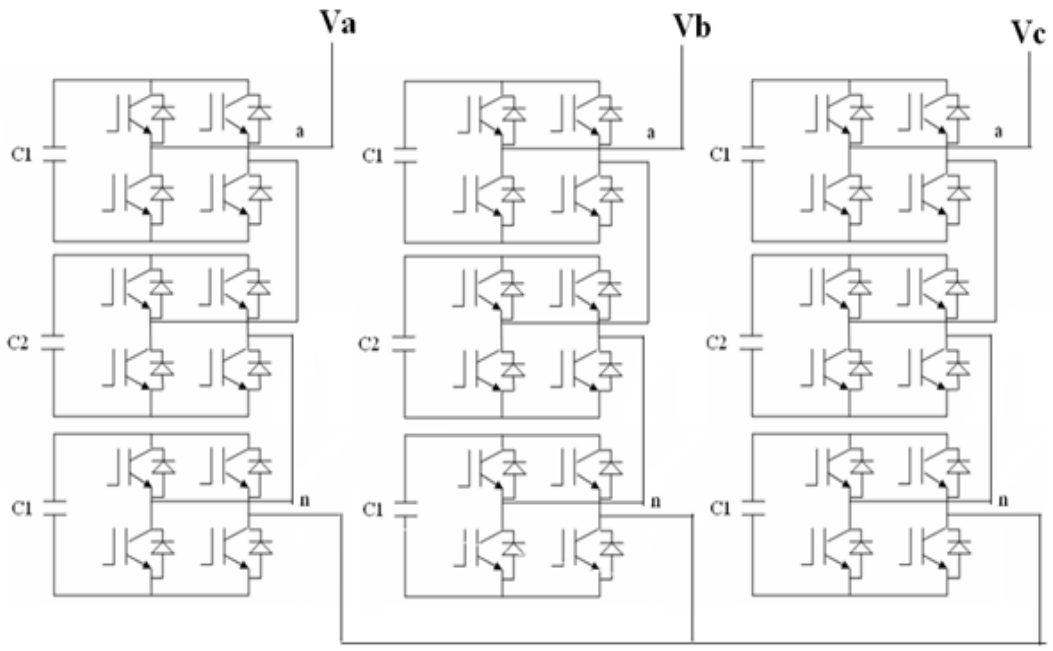

Fig 2.6 Three-phase 7-level cascaded multilevel inverter (Y-configuration)

2.3.2 Features of CMLI

For real power conversions, (ac to dc and dc to ac), the cascaded-inverter needs separate dc sources. The structure of separate dc sources is well suited for various renewable energy sources such as fuel cell, photovoltaic, and biomass, etc.

Connecting separated dc sources between two converters in a back-to-back fashion is not possible because a short circuit will be introduced when two back-to-back converters are not switching synchronously.

In summary, advantages and disadvantages of the cascaded inverter based multilevel voltage source converter can be listed below.

2.3.3 Advantages and Disadvantages of CMLI.

Advantages

i) The regulation of the DC buses is simple.

ii) Modularity of control can be achieved. Unlike the diode clamped and capacitor clamped inverter where the individual phase legs must be modulated by a central controller, the full-bridge inverters of a cascaded structure can be modulated separately.

iii) Requires the least number of components among all multilevel converters to achieve the same number of voltage levels.

iv) Soft-switching can be used in this structure to avoid bulky and lossy resistor-capacitor-diode snubbers.

Disadvantages

i) Communication between the full-bridges is required to achieve the synchronization of reference and the carrier waveforms.

ii) Needs separate dc sources for real power conversions, and thus its applications are somewhat limited

2.4 Conclusion

The aim of this chapter has been to demonstrate the multilevel converter topologies. Each has its own mixture of advantages and disadvantages and for any one particular application, one topology will be more appropriate than the others. Often, topologies are chosen based on what has gone before, even if that topology may not be the best choice for the application. The advantages of the body of research and familiarity within the engineering community may out weight other technical disadvantages.

Chapter 3

MODULATION TECHNIQUES FOR MULTILEVEL INVERTER

A Definition of Modulation

PWM Techniques

Carrier-Based PWM Schemes

3.1 A Definition of Modulation.

Mainly the power electronic converters are operated in the "switched mode". Which means the switches within the converter are always in either one of the two states - turned off (no current flows), or turned on (saturated with only a small voltage drop across the switch). Any operation in the linear region, other than for the unavoidable transition from conducting to non-conducting, incurs an undesirable loss of efficiency and an unbearable rise in switch power dissipation. To control the flow of power in the converter, the switches alternate between these two states (i.e. on and off). This happens rapidly enough that the inductors and capacitors at the input and output nodes of the converter average or filter the switched signal. The switched component is attenuated and the desired DC or low frequency AC component is retained. This process is called Pulse Width Modulation (PWM), since the desired average value is controlled by modulating the width of the pulses.

For maximum attenuation of the switching component, the switch frequency *fc* should be high- many times the frequency of the desired fundamental AC component f_1 seen at the input or output terminals. In large converters, this is in conflict with an upper limit placed on switch frequency by switching losses. For GTO converters, the ratio of switch frequency to fundamental frequency f_c/f_1 (= N, the pulse number) may be as low as unity, which is known as square wave switching. Another application where the pulse number may be low is in converters which are better described as amplifiers [39], whose upper output fundamental frequency may be relatively high. These high power switch-mode amplifiers find application in active power filtering [40], test signal generation [41], servo [42] and audio amplifiers [43]. These low pulse numbers place the greatest demands on effective modulation to reduce the distortion as much as possible.

The low pulse numbers place the greatest demands on effective modulation to reduce the distortion as much as possible. In these circumstances, multi-level converters can reduce the distortion substantially, by staggering the switching instants of the multiple switches and increasing the apparent pulse number of the overall converter.

3.2 PWM Techniques

The fundamental methods of pulse-width modulation (PWM) are divided into the traditional voltage-source and current-regulated methods. Voltage-source methods more easily lend themselves to digital signal processor (DSP) or programmable logic device (PLD) implementation. However, current controls typically depend on event scheduling and are therefore analog implementations which can only be reliably operated up to a certain power level. In discrete current-regulated methods the harmonic performance is not as good as that of voltage-source methods. A sample PWM method is described below.

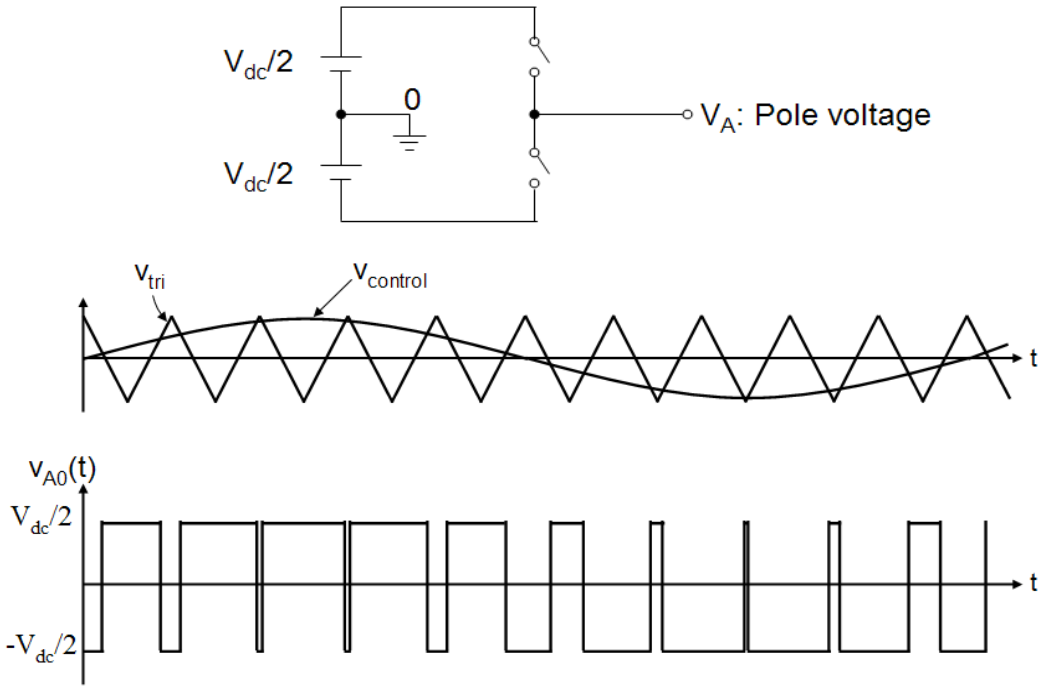

Fig. 3.1 Pulse-width modulation.

Inverter output voltage, $V_{A0} = V_{dc}/2$, When $v_{control} > v_{tri,}$ and $V_{A0} = -V_{dc}/2$, When $v_{control} < v_{tri}$.

PWM frequency is the same as the frequency of v_{tri} . Amplitude is controlled by the peak value of $v_{control}$ and Fundamental frequency is controlled by the frequency of $v_{control}$.

Modulation Index (m) is given by :

$$m = \frac{v_{control}}{v_{tri}} = \frac{peak \quad of \quad (V_{A0})_1}{V_{dc}/2}, \tag{3.1}$$

Where $(V_{A0})_1$ is the fundamental frequency component of V_{A0}

3.2.1 Voltage-source methods

Voltage-source modulation has taken two major paths; sine triangle modulation in the time domain and space vector modulation in the q-d stationary reference frame. Sine-triangle and space vector modulation are exactly equivalent in every way. Adjusting some parameters in the sine-triangle scheme (such as the triangle shape and sine wave harmonics) is equivalent to adjusting other parameters in the space vector scheme (such as the switching sequence and dwell time).

The inverter line-to-ground voltage can be directly controlled through the switching state. For a specific inverter, the switching state is broken out into transistor signals. However, as a control objective, it is more desirable to regulate the line-to-neutral voltages of the load. In a three-phase system, the common terms include dc offset and any triplen harmonics. To narrow the possibilities, the commanded line-to-ground voltages will be defined herein as:

$$\begin{bmatrix} Vag* \\ Vbg* \\ Vcg* \end{bmatrix} = \frac{mVdc}{2}\begin{bmatrix} \cos(\theta c) \\ \cos(\theta c - \frac{2\pi}{3}) \\ \cos(\theta c + \frac{2\pi}{3}) \end{bmatrix} + \frac{Vdc}{2}\left[1 - \frac{m}{6}\cos(3\theta c)\right]\begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} \qquad (3.2)$$

where *m* is the modulation index which has a range of $0 \leq m \leq \frac{2}{\sqrt{3}}$ and θc the converter electrical angle.

In eqn. 3.2, first set of terms on the right hand side define a sinusoidal set of commanded voltages with controllable amplitude and frequency through *m* and θc respectively. The second set of terms on the right hand side is the common-mode terms. In this case, a dc offset is applied so that the commanded line-to-ground voltages will be within the allowable range of zero to the dc voltage. The other common-mode term is a third harmonic component which is added to fully utilize the dc source voltage. The common-mode terms are just the minimum set and it is possible to command other types of line-to-ground voltages, including discontinuous waveforms, in order to optimize switching frequency or harmonics.

Some fundamental definitions will now be presented for reference when describing the modulation methods. First, duty cycles are defined by scaling the commanded voltages with modifications to account for multiple voltage levels. The modified duty cycles are-

$$\begin{bmatrix} d_{am} \\ d_{bm} \\ d_{cm} \end{bmatrix} = \left(\frac{n-1}{2}\right)\begin{bmatrix} m\cos(\theta c) \\ m\cos(\theta c - \frac{2\pi}{3}) \\ m\cos(\theta c + \frac{2\pi}{3}) \end{bmatrix} + \left(\frac{n-1}{2}\right)\left[1 - \frac{m}{6}\cos(3\theta c)\right]\begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} \qquad (3.3)$$

Next, a commanded voltage vector is defined by

$$v^{s*}_{qds} = v^{s*}_{qs} - jv^{s*}_{ds} \tag{3.4}$$

where the commanded *q*- and *d*-axis voltages are related to the *a*-*b*-*c* variables of eqn.3.2

$$v^{s*}_{qs} = \frac{2}{3}v^{*}_{ag} - \frac{1}{3}v^{*}_{bg} - \frac{1}{3}v^{*}_{cg} \tag{3.5}$$

$$v^{s*}_{ds} = \frac{1}{\sqrt{3}}(v^{*}_{cg} - v^{*}_{bg}) \tag{3.6}$$

It should be pointed out that the commanded *q*- and *d*-axis voltages can also be defined in terms of desired line-to-neutral voltages since the zero sequence is being ignored.

(I) Sine-triangle modulation

In sine-triangle method, therein, for n-level inverter the *a*-phase duty cycle is compared with (*n*-1 in general) triangle waveforms. The switching rules are as follows:

$$s_{ai} = \begin{cases} 1 & d_{am} \succ tri \\ 0 & elsewise \end{cases} \tag{3.7}$$

$$Sa = \sum_{i=1}^{n-1} Sai \tag{3.8}$$

In general the sine triangle modulation is discussed here for a 3-phase inverter.

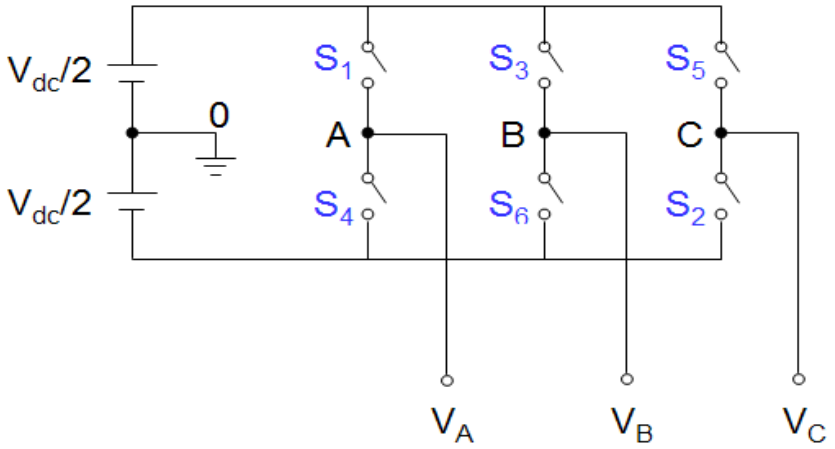

Fig. 3.2 Three-phase Sinusoidal PWM inverter

One of the methods of describing voltage-source modulation is to illustrate the intersection of a modulating signal (duty cycle) with triangle waveforms.

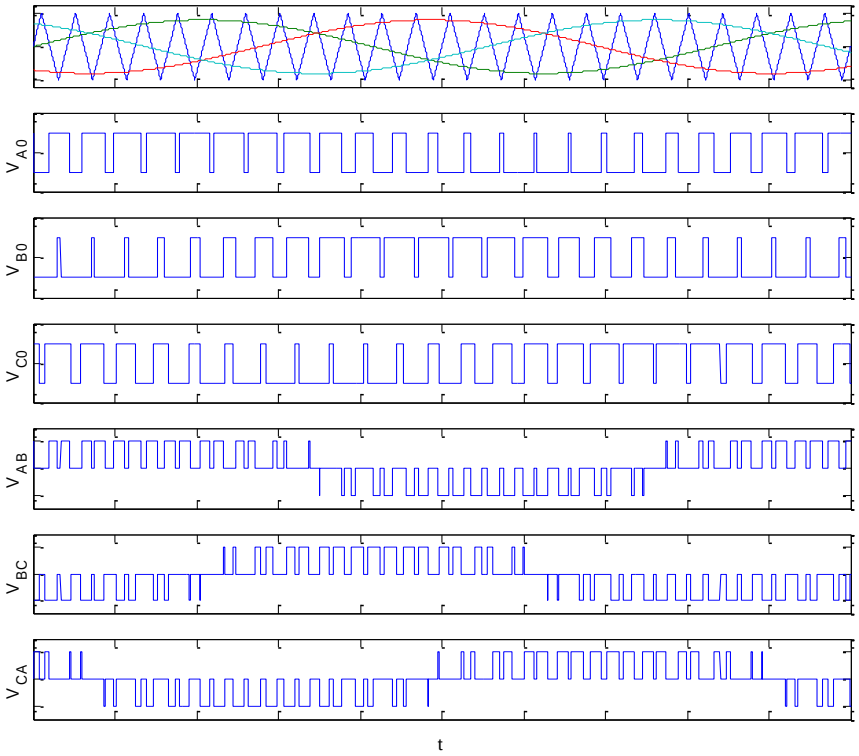

Fig. 3.3 Waveforms of three-phase SPWM inverter.

Let, frequency of $v_{tri} = f_s$ = PWM frequency and frequency of $v_{control} = f_1$ = fundamental frequency.In the above figure $V_{AB} = V_{A0} - V_{B0}$, $V_{BC} = V_{B0} - V_{C0}$and $V_{CA} = V_{C0} - V_{A0}$

Amplitude modulation ratio (m_a) is given by :

$$\therefore m_a = \frac{peak \quad amplitude \quad of \quad v_{control}}{amplitude \quad of \quad v_{tri}} = \frac{peak \quad value \quad of \quad (V_{A0})_1}{V_{dc}/2},$$

where, $(V_{A0})_1$:fundamental frequecny component of V_{A0}

Frequency modulation ratio (m_f) can be expressed as :

$$m_f = \frac{f_s}{f_1}, \quad \text{where,} \quad f_s = \text{PWM} \quad \text{frequency} \quad \text{and} \quad f_1 = \text{fundamental} \quad \text{frequency}$$

m_f should be an odd integer. If m_f is not an integer, there may exist sub harmonics at output voltage. If m_f is not odd, DC component may exist and even harmonics are present at output voltage. m_f should be a multiple of 3 for three-phase PWM inverter.

The carrier-based modulation schemes for multilevel inverters can be generally classified into two categories: phase-shifted and level-shifted modulations. Both modulation schemes can be applied to the cascaded H-bridge(CHB) inverters.THD of phase-shifted modulation is much higher than level-shifted modulation. Therefore we have considered level-shifted modulation. An m-level CHB inverter using level-shifted multicarrier modulation scheme requires (m-1) triangular carriers, all having the same frequency and amplitude. The (m-1) triangular carriers are vertically disposed such that the bands they occupy are contiguous. There are three alternative PWM strategies with different phase relationships for the level-shifted multicarrier modulation:

(i) In-phase disposition (IPD), where all carrier waveforms are in phase.

(ii) Phase opposition disposition (POD), where all carrier waveforms above zero reference are in phase and are 180^0 out of phase with those below zero.

(iii) Alternate phase disposition (APOD), where every carrier waveform is in out of phase with its neighbor carrier by 180^0.

(a) In Phase Disposition (IPD)

In the present work, in the carrier-based implementation the phase disposition PWM scheme is used. Figure 3.4 demonstrates the sine-triangle method for a three-level inverter. Therein, the a-phase modulation signal is compared with two (n-1 in general) triangle waveforms.

The rules for the in phase disposition method, when the number of level N = 3, are

• The N –1 = 3-1=2 carrier waveforms are arranged so that every carrier is in phase.

• The converter is switched to $+V_{dc}/ 2$ when the reference is greater than both carrier waveforms.

• The converter is switched to zero when the reference is greater than the lower carrier waveform but less than the upper carrier waveform.

• The converter is switched to $- V_{dc}/ 2$ when the reference is less than both carrier waveforms.

In the carrier-based implementation, at every instant of time the modulation signals are compared with the carrier and depending on which is greater, the switching pulses are generated. As seen from Figure 3.4, the figure illustrates the switching pattern produced by the carrier-based PWM scheme. In the PWM scheme there are two triangles, the upper triangle ranges from 1 to 0 and the lower triangle ranges from 0 to –1. In the similar way for an N –level inverter, the (N-1) triangles are used and each has a peak-to-peak value of 2/ (N-1). Hence the upper most triangle magnitude varies from 1 to (1-2/ (N-1)), second carrier waveform from (1-4/ (N-1)), and the bottom most triangle varies from (2-2/ (N-1)) to –1. In Figure 3.5, simulation of carrier-based

PWM scheme using the in phase disposition (IPD) can be seen. The switching function for the devices is given by

H_a > Triangle -1 & Triangle -2; H_{a3} =1, otherwise H_{a3} =0.

H_a < Triangle -1 & Ha > Triangle -2; H_{a2} =1, otherwise H_{a2} =0.

H_a < Triangle -1 & Triangle -2; H_{a1} =1, otherwise H_{a1} =0.

It is clear from the figure that during the positive cycle of the modulation signal, when the modulation is greater than Triangle 1 and Triangle 2, then S_{1ap} and S_{2ap} are turned on and also during the positive cycle S_{2ap} is completely turned on. When S_{1ap} and S_{2ap} are turned on, the converter switches to the + V_{dc} / 2.When S_{1an} and S_{2ap} are on, the converter switches to zero and hence during the positive cycle S_{2ap} is completely turned on and S_{1ap} and S_{1an} will be turning on and off and hence the converter switches from + V_{dc} / 2 to 0.During the negative half cycle of the modulation signal the converter switches from 0 to - V_{dc} / 2. The phase voltage equations for star-connected, balanced three-phase loads expressed in terms of the existence functions and input nodal voltage $V_{30} = V_{dc} / 2$, $V_{20} = 0$, $V_{10} = -V_{dc} / 2$.

$V_{a0} = H_{a3}V_{30} + H_{a2}V_{20} + H_{a1}V_{10}$.

$V_{b0} = H_{b3}V_{30} + H_{b2}V_{20} + H_{b1}V_{10}$.

$V_{c0} = H_{c3}V_{30} + H_{c2}V_{20} + H_{c1}V_{10}$.

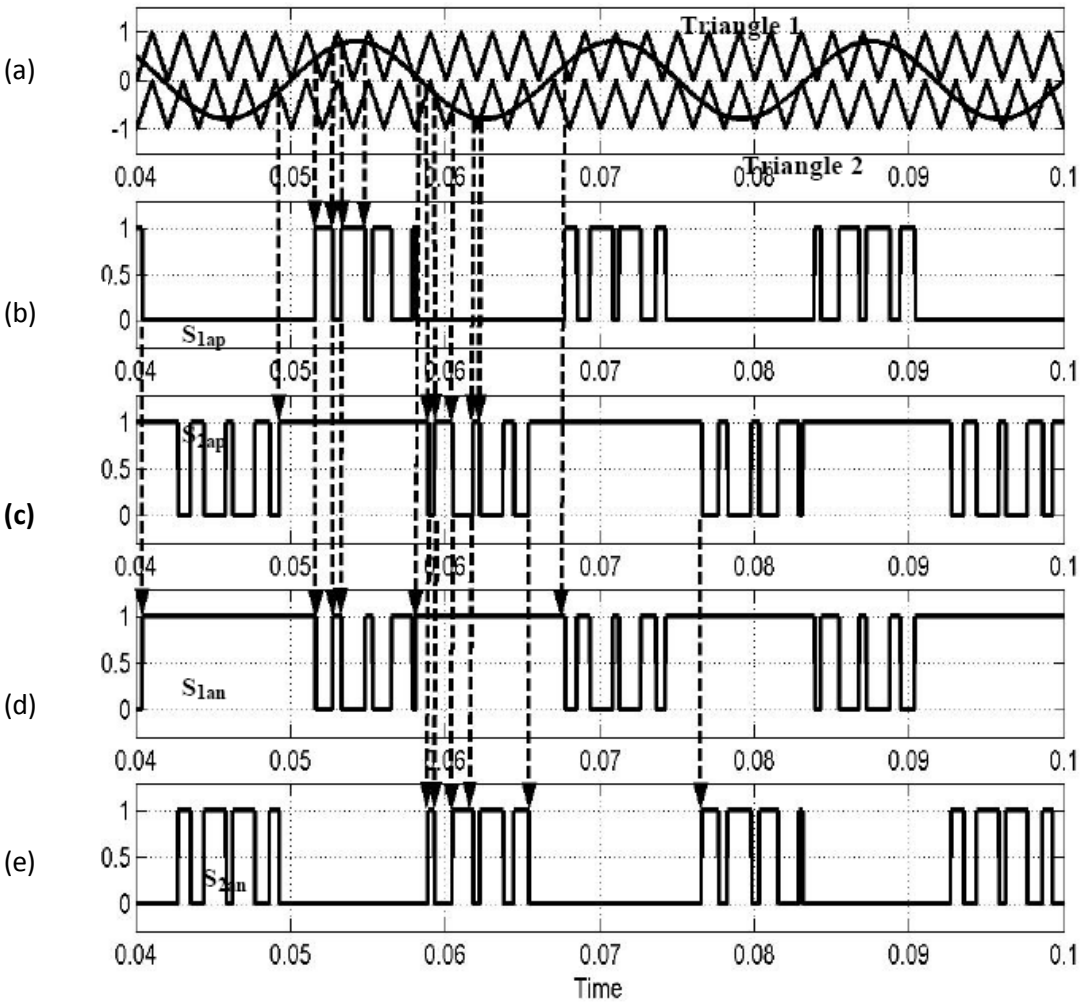

Fig.3.4: Switching pattern produced using the IPD carrier-based PWM scheme: (a) two triangles and the modulation signal (b) S_{1ap} (c) S_{2ap} (d) S_{1an} (e) $S_{2an.}$

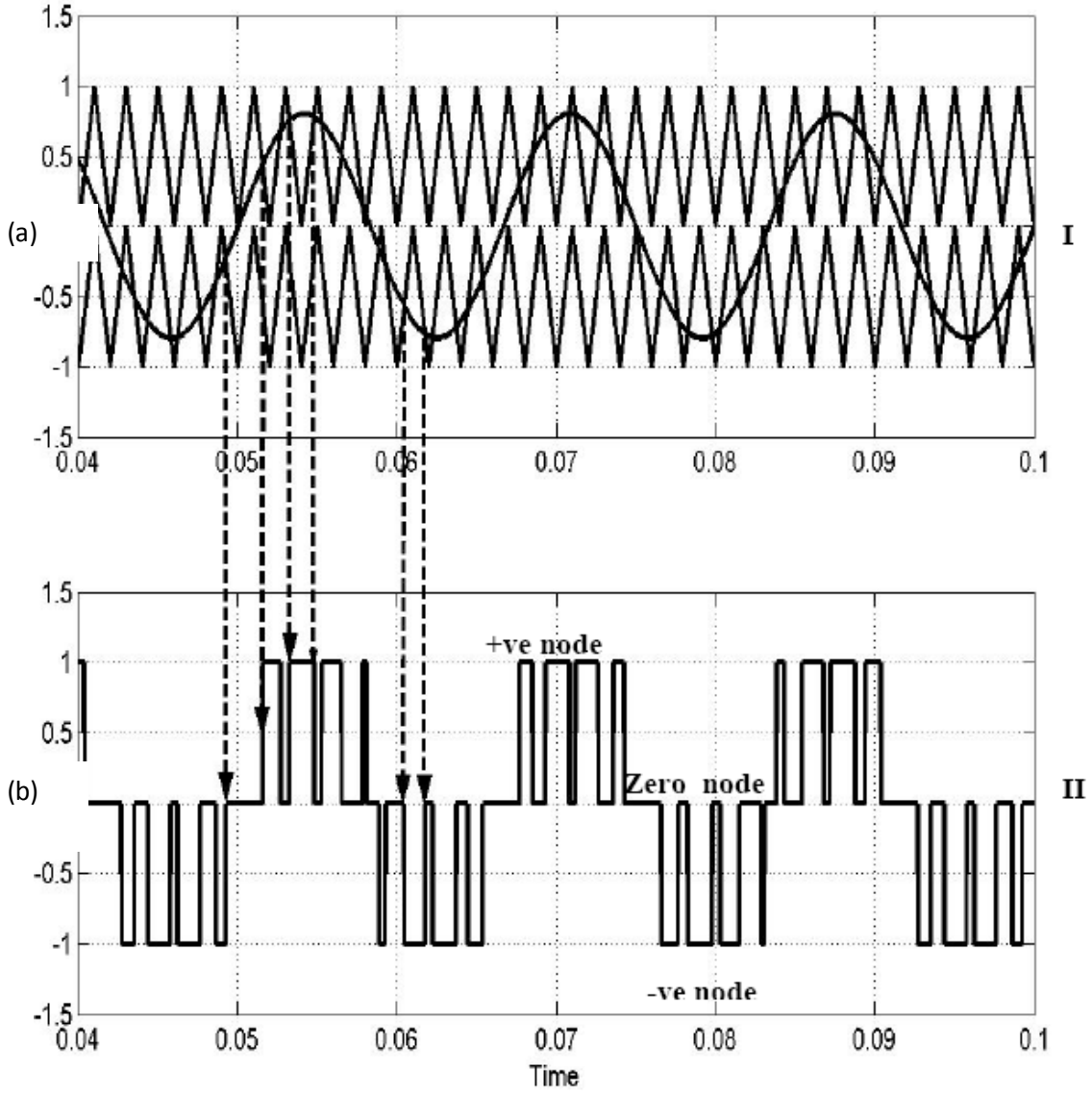

Fig. 3.5: Simulation of carrier-based PWM scheme using the in phase disposition (IPD). (a). Modulation signal and in-phase carrier waveforms (b) Phase "a" output voltage.

(b) Phase Opposition Disposition (POD).

For phase opposition disposition (POD) modulation all carrier waveforms above zero reference are in phase and are 180^0 out of phase with those below zero. The rules for the phase opposition disposition method, when the number of level N = 3 are

(i) The N –1 = 2 carrier waveforms are arranged so that all carrier waveforms above zero are in phase and are 180^{0} out of phase with those below zero.

(ii) The converter is switched to + V_{dc} / 2 when the reference is greater than both carrier waveforms.

(iii) The converter is switched to zero when the reference is greater than the lower carrier waveform but less than the upper carrier waveform.

(iv) The converter is switched to - Vdc / 2 when the reference is less than both carrier waveforms.

As seen from Figure 3.6, the figure illustrates the switching functions produced by POD carrier-based PWM scheme. In the PWM scheme there are two triangles, upper triangle magnitude from 1 to 0 and the lower triangle from 0 to –1 and these two triangle waveforms are in out of phase. When the modulation signal is greater than both the carrier waveforms, S_{1ap} and S_{2ap} are turned on and the converter switches to positive node voltage and when the reference is less than the upper carrier waveform but greater than the lower carrier, S_{2ap} and S_{1an} are turned on and the converter switches to neutral point. When the reference is lower than both carrier waveforms, S_{1an} and S_{2an} are turned on and the converter switches to negative node voltage. . Figure 3.7 shows the output voltage waveform of phase “a” and it is clear the waveform has three steps.

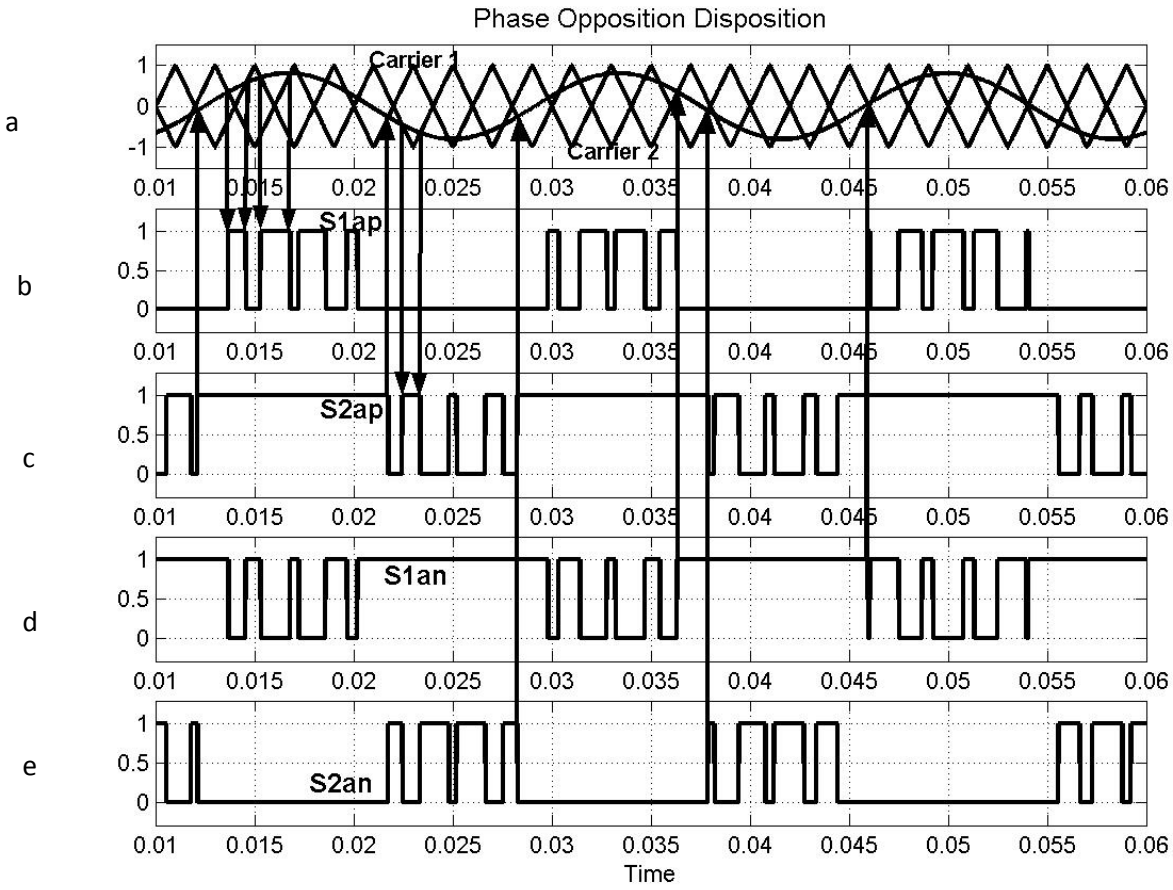

Fig. 3.6: Switching pattern produced using the POD carrier-based PWM scheme: (a) two triangles and the modulation signal (b) S_{1ap} (c) S_{2ap} (d) S_{1an} (e) $S_{2an.}$

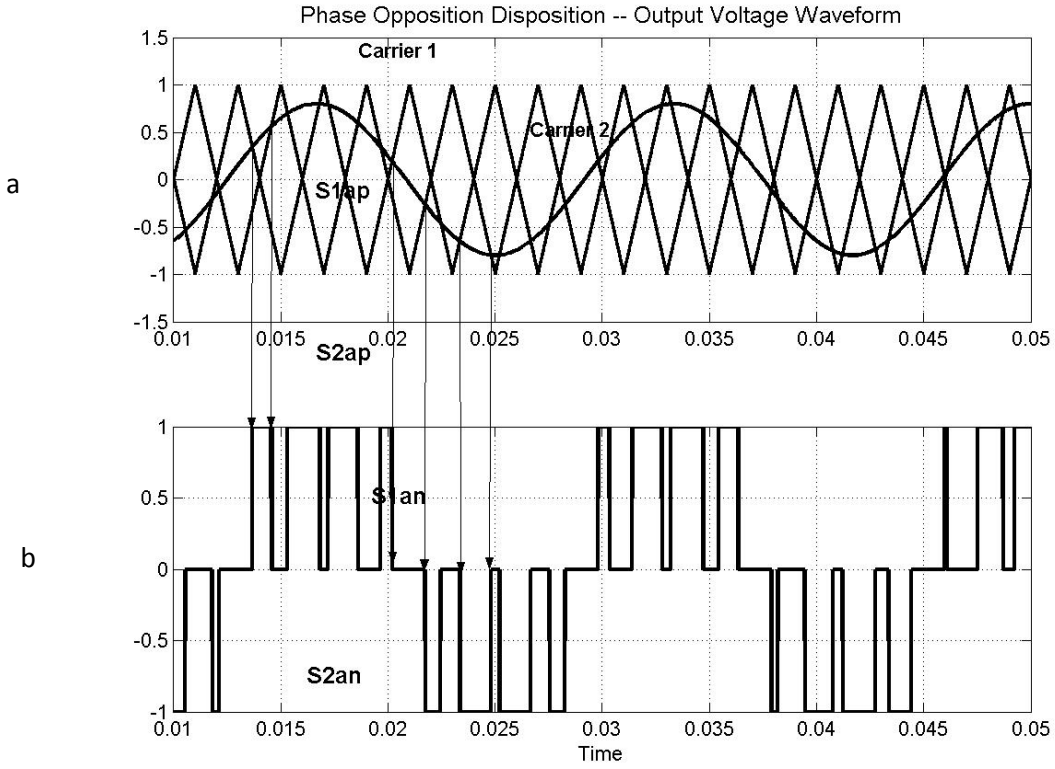

Fig.3.7: Simulation of carrier-based PWM scheme using POD. (a). Modulation signal and phase carrier waveforms (b) Phase "a" output voltage.

(c) Alternate Phase Opposition Disposition (APOD).

In case of alternate phase disposition (APOD) modulation, every carrier waveform is in out of phase with its neighbor carrier by 180^0. Since APOD and POD schemes in case of three-level inverter are the same, a five level inverter is considered to discuss about the APOD scheme.

The rules for APOD method, when the number of level N = 5, are

i) The N – 1 = 4 carrier waveforms are arranged so that every carrier waveform is in out of phase with its neighbor carrier by 180^0. The converter switches to + V_{dc} / 2 when the reference is greater than all the carrier waveforms.

(ii) The converter switches to V_{dc} / 4 when the reference is less than the uppermost carrier waveform and greater than all other carriers.

(iii) The converter switches to 0 when the reference is less than the two uppermost carrier waveform and greater than two lowermost carriers.

(iv) The converter switches to - V_{dc} / 4 when the reference is greater than the lowermost carrier waveform and lesser than all other carriers.

(v) The converter switches to -V_{dc} / 2 when the reference is lesser than all the carrier waveforms.

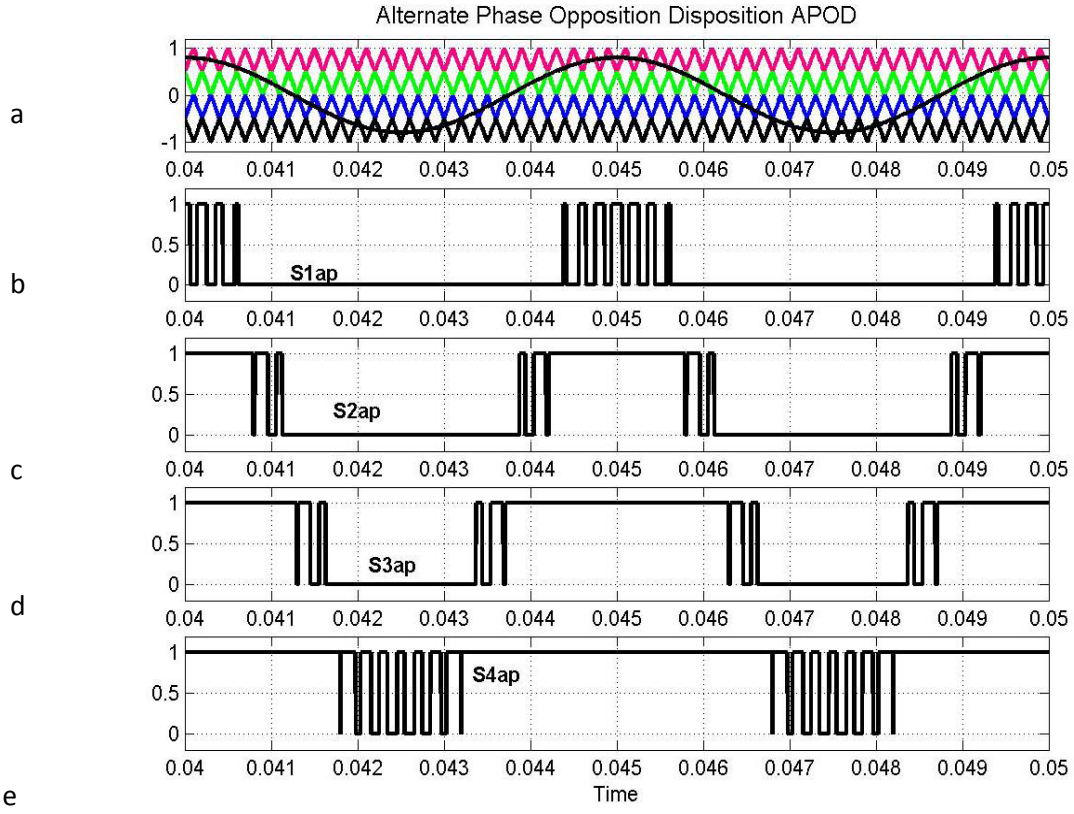

Fig. 3.8: Switching pattern produced using the APOD carrier-based PWM scheme for a five-level inverter: (a) Four triangles and the modulation signal (b) S_{1ap} (c) S_{2ap} (d) S_{3ap} (e) $S_{4ap.}$

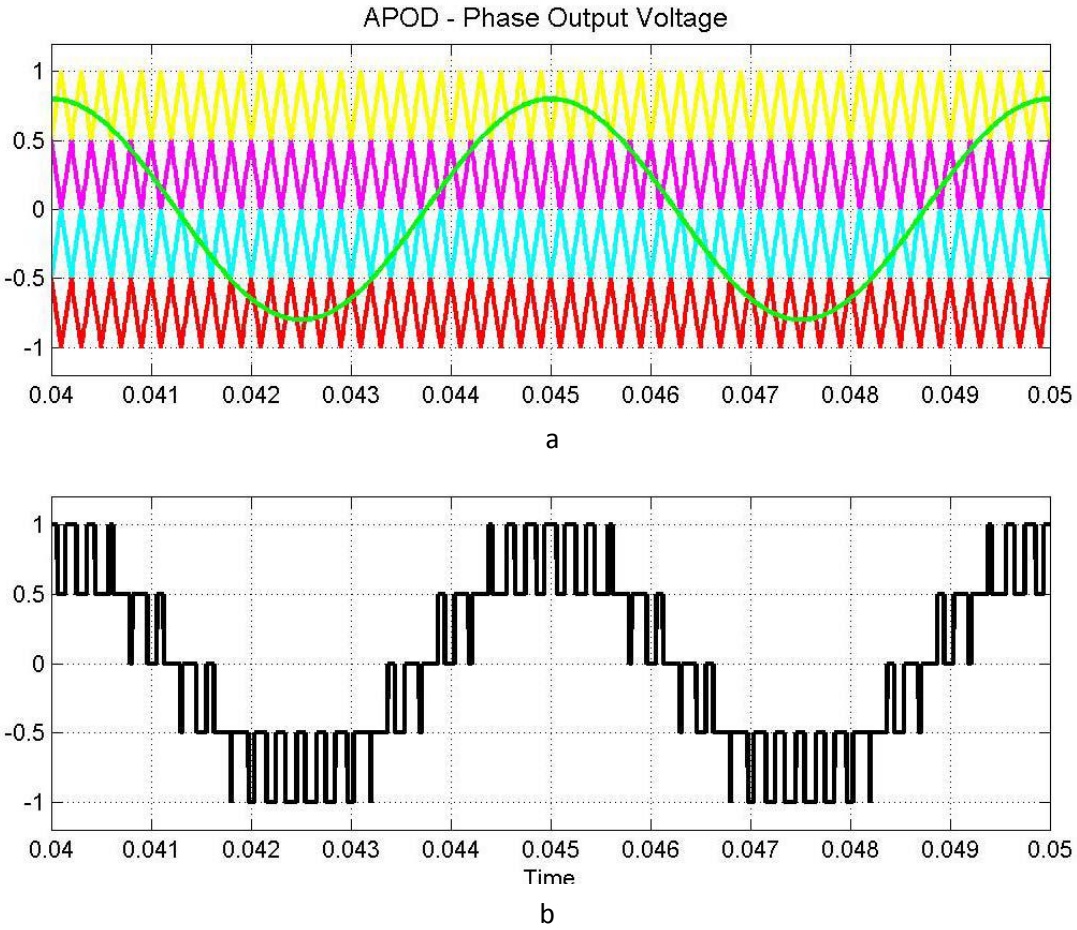

Fig.3.9: Simulation of carrier-based PWM scheme using APOD for a five-level inverter. (a) Modulation signal and carrier waveforms (b) Phase "a" output voltage.

Figure 3.8 demonstrates the APOD scheme for a five-level inverter. The figure displays the switching pattern generated by the comparison of the modulation signals with the four carrier waveforms. Figure 3.9 shows the output voltage waveform of phase "a" and it is clear the waveform has five steps.

II. Space vector modulation

Space vector modulation (SVM) is based on vector selection in the q-d stationary reference frame. The commanded voltage vector is defined by equation-3.5. The commanded vector is plotted along with the vectors obtainable by the inverter. The desired vector V^{s*}_{qds} is

shown at some point in time, but will follow the circular path if a three-phase set of voltages are required on the load. The first step in the SVM scheme is to identify the three nearest vectors.

(i)Realization of Space Vector PWM

Step -1 Determine V_d, V_q, V_{ref}, and angle (α)

Step -2 Determine time duration T_1, T_2, T_0

Step -3 Determine the switching time of each transistor (S_1 to S_6)

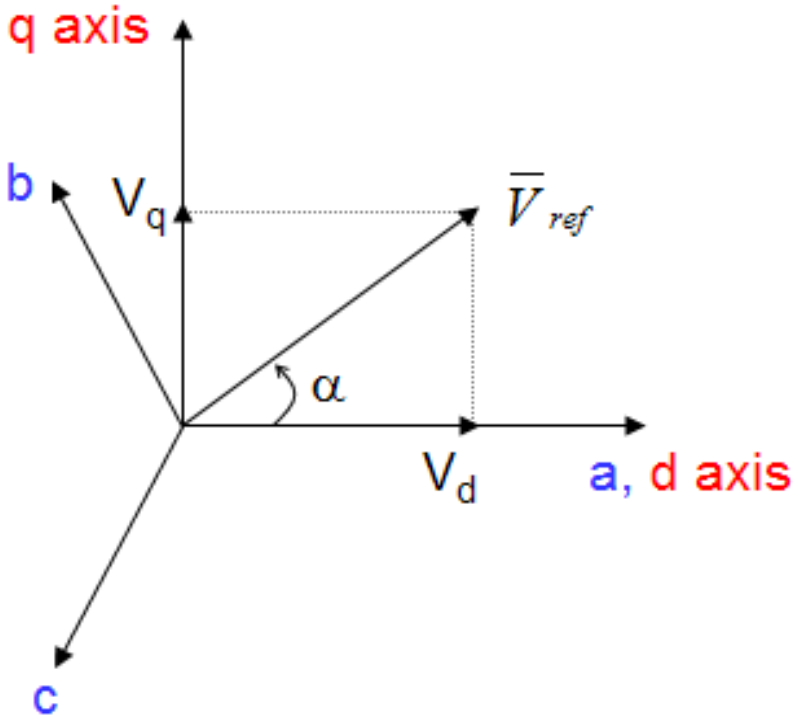

Fig. 3.10 Voltage Space Vector and its components in (d, q).

(ii) Coordinate transformation: abc to dq

$$V_d = V_{an} - V_{bn} \cdot \cos 60 - V_{cn} \cdot \cos 60 = V_{an} - \frac{1}{2} V_{bn} - \frac{1}{2} V_{cn} \tag{3.9}$$

$$V_q = 0 + V_{bn} \cdot \cos 30 - V_{cn} \cdot \cos 30 = V_{an} + \frac{\sqrt{3}}{2} V_{bn} - \frac{\sqrt{3}}{2} V_{cn} \tag{3.10}$$

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} \tag{3.11}$$

$$\left| \overline{V}_{ref} \right| = \sqrt{V_d^{\,2} + V_q^{\,2}} \tag{3.12}$$

$$\alpha = \tan^{-1}\left(\frac{V_q}{V_d}\right) = \omega_s t = 2\pi f_s t \tag{3.13}$$

Where, f_s = fundamental frequency

Switching time duration at Sector 1 is described below

$$\int_0^{T_z} \overline{V}_{ref} = \int_0^{T_1} \overline{V}_1 dt + \int_{T1}^{T_1+T_2} \overline{V}_2 dt + \int_{T_1+T_2}^{T_z} \overline{V}_0 \tag{3.14}$$

$$T_z \cdot \overline{V}_{ref} = (T_1 \cdot \overline{V}_1 + T_2 \cdot \overline{V}_2) \tag{3.15}$$

$$T_z \cdot \left| \overline{V}_{ref} \right| \cdot \begin{bmatrix} \cos(\alpha) \\ \sin(\alpha) \end{bmatrix} = T_1 \cdot \frac{2}{3} \cdot V_{dc} \cdot \begin{bmatrix} 1 \\ 0 \end{bmatrix} + T_2 \cdot \frac{2}{3} \cdot V_{dc} \cdot \begin{bmatrix} \cos(\pi/3) \\ \sin(\pi/3) \end{bmatrix} \tag{3.16}$$

where $0 \leq \alpha \leq 60^\circ$

$$T_1 = T_z \cdot a \cdot \frac{\sin(\pi/3 - \alpha)}{\sin(\pi/3)} \tag{3.17}$$

$$T_2 = T_z \cdot a \cdot \frac{\sin(\alpha)}{\sin(\pi/3)} \tag{3.18}$$

$$T_0 = T_z - (T_1 + T_2), \quad \left(\text{where,} \quad T_z = \frac{1}{f_s} \quad \text{and} \quad a = \frac{\left|\bar{V}_{ref}\right|}{\frac{2}{3} V_{dc}} \right) \tag{3.19}$$

Switching time duration at any Sector is shown below

$$T_1 = \frac{\sqrt{3} T_z \cdot \left|\bar{V}ref\right|}{V_{dc}} \left(\sin\left(\frac{\pi}{3} - \alpha + \frac{n-1}{3}\pi \right) \right) = \frac{\sqrt{3} \cdot T_z \cdot \left|\bar{V}ref\right|}{V_{dc}} \left(\sin \frac{n}{3}\pi - \alpha \right)$$

$$= \frac{\sqrt{3} \cdot T_z \cdot \left|\bar{V}ref\right|}{V_{dc}} \left(\sin \frac{n}{3}\pi \cos\alpha - \cos \frac{n}{3}\pi \sin\alpha \right) \tag{3.20}$$

$$T_2 = \frac{\sqrt{3} \cdot T_z \cdot \left|\bar{V}ref\right|}{V_{dc}} \left(\sin\left(\alpha - \frac{n-1}{3}\pi \right) \right)$$

$$= \frac{\sqrt{3} \cdot T_z \left|\bar{V}ref\right|}{V_{dc}} \left(-\cos\alpha \cdot \sin \frac{n-1}{3}\pi + \sin\alpha \cdot \cos \frac{n-1}{3}\pi \right) \tag{3.21}$$

$$T_0 = T_z - T_1 - T_2 \tag{3.22}$$

Where, n=1 through 6 (that is sector 1 to 6),$0 \le \alpha \le 60^{\circ}$

A three-phase Power inverter is shown below

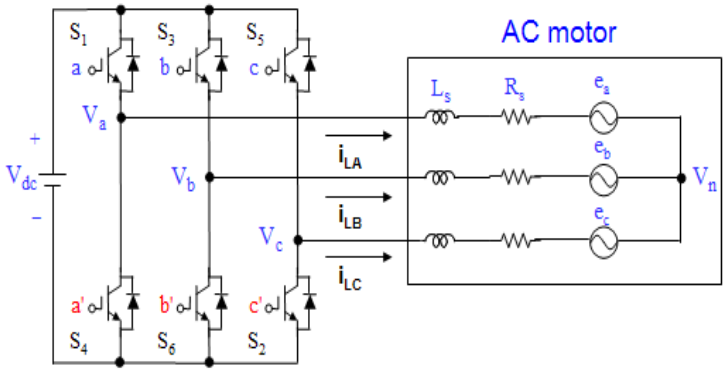

Fig. 3.11 Three-phase Power inverter

The upper transistors are S_1, S_3, S_5, lower transistors: S_4, S_6, S_2 and switching variable vectors are a, b, c. The switching time of each transistor (S_1 to S_6) is shown below in Table-1

Table-3.1 Switching Time Table at Each Sector in SVM

Sector	Upper Switches(S1,S3,S5)	Lower switches(S4,S6,S2)
1	$S_1=T_1+T_2+T_{0/2}$ $S_3=T_2+T_{0/2}$ $S_5=T_{0/2}$	$S_4=T_{0/2}$ $S_6=T_1+T_{0/2}$ $S_2=T_1+T_2+T_{0/2}$
2	$S_1=T_1+T_{0/2}$ $S_3=T_1+T_2+T_{0/2}$ $S_5=T_{0/2}$	$S4=T_2+T_{0/2}$ S6=T0/6 $S2=T_1+T_2+T_{0/2}$
3	$S_1=T_{0/2}$ $S_3=T_1+T_2+T_{0/2}$ $S_5=T2+T_{0/2}$	$S4=T_1+T_2+T_{0/2}$ $S6=T_{0/2}$ $S2=T_1+T_{0/2}$
4	$S_1=T_{0/2}$ $S_3=T_1+T_{0/2}$ $S_5=T_1+T_2+T_{0/2}$	$S4=T_1+T_2+T_{0/2}$ $S6=T_2+T_{0/2}$ $S2=T_{0/2}$
5	$S_1=T_2+T_{0/2}$ $S_3=T_{0/2}$ $S_5=T_1+T_2+T_{0/2}$	$S4=T_1+T_{0/2}$ $S6=T_1+T_2+T_{0/2}$ $S2=T_{0/2}$
6	$S_1=T_1+T_2+T_{0/2}$ $S_3=T_{0/2}$ $S_5=T_1+T_{0/2}$	$S4=T_{0/2}$ $S6=T_1+T_2+T_{0/2}$ $S2=T_2+T_{0/2}$

(iii) Output voltages of three-phase inverter

S_1 through S_6 are the six power transistors that shape the output voltage. When an upper switch is turned on (i.e., a, b or c is "1"), the corresponding lower switch is turned off (i.e., a', b' or c' is "0").Eight possible combinations of on and off patterns for the three upper transistors (S_1, S_3, S_5) are possible.

Line to line voltage vector $[V_{ab}\ V_{bc}\ V_{ca}]^t$. Where voltage vectors are [a, b, c]

$$\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = V_{dc} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \quad (3.23)$$

Line to neutral (phase) voltage vector $[V_{an}\ V_{bn}\ V_{cn}]^t$

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = \frac{1}{3} V_{dc} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \tag{3.24}$$

The eight inverter voltage vectors (V_0 to V_7) are shown below in figure 3.12.

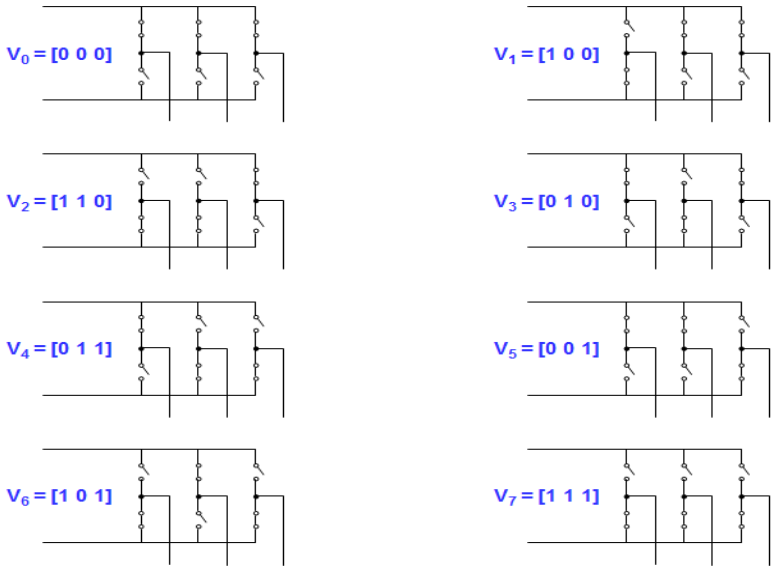

Fig. 3.12 Inverter voltage vectors

The eight combinations, phase voltages and output line to line voltages are shown below in table-3.2

Table-3.2 Phase voltages and output line to line voltages in SVM

Voltage Vectors	Switching Vectors			Line to neutral voltage			Line to line voltage		
	a	b	c	Van	Vbn	Vcn	Vab	Vbc	Vca
Vo	0	0	0	0	0	0	0	0	0
V1	1	0	0	2/3	-1/3	-1/3	1	0	-1
V2	1	1	0	1/3	1/3	-2/3	0	1	-1
V3	0	1	0	-1/3	2/3	-1/3	-1	1	0
V4	0	1	1	-2/3	1/3	1/3	-1	0	1
V5	0	0	1	-1/3	-1/3	2/3	0	-1	1
V6	1	0	1	1/3	-2/3	1/3	1	-1	0
V7	1	1	1	0	0	0	0	0	0

(iv) Principle of Space Vector PWM

a. Treats the sinusoidal voltage as a constant amplitude vector rotating at constant frequency

b. This PWM technique approximates the reference voltage V_{ref} by a combination of the eight switching patterns (V_0 to V_7)

c. Coordinate Transformation (abc reference frame to the stationary d-q frame) : A three-phase voltage vector is transformed into a vector in the stationary d-q coordinate frame which represents the spatial vector sum of the three-phase voltage

d. The vectors (V_1 to V_6) divide the plane into six sectors (each sector: 60 degrees)

e. V_{ref} is generated by two adjacent non-zero vectors and two zero vectors

(v) Basic switching vectors and Sectors

6 active vectors are (V_1, V2, V_3, V_4, V_5, V_6) .DC link voltage is supplied to the load. Each sector (1 to 6): 60 degrees.Two zero vectors are (V_0, V_7). They are located at origin. No voltage is supplied to the load.

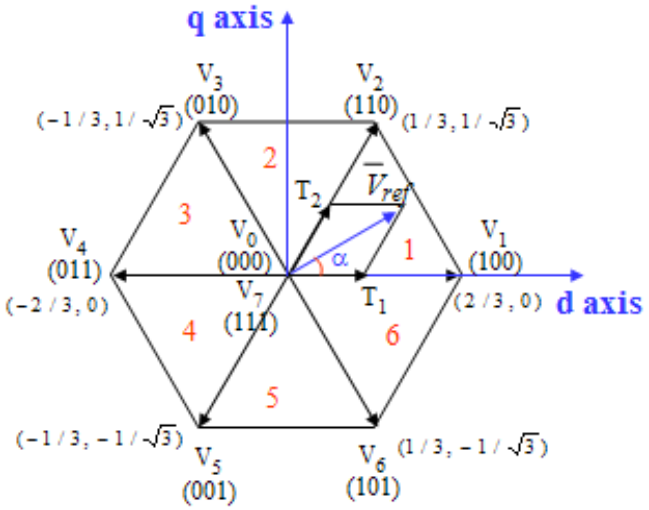

Fig.3.13 Basic switching vectors and sectors.

(III) Discrete implementation

One attractive feature of voltage-source PWM methods is that they can be readily implemented on a DSP/PLD control. In a per-phase time domain method of implementing PWM in a discrete time system, the modified phase duty cycle is shown along with the switching state output of the modulator. At each point in time, the phase duty cycle is updated based on the magnitude and phase of the commanded voltages. In a DSP system, discrete values of the duty cycle are computed which are represented by points. This creates a zero order- hold effect which is negligible if the switching frequency is large compared to the changes in the duty cycle. In order to schedule the switching state transitions during the switching period, the nearest lower and upper voltage levels are determined. Next, a switching time for each phase is determined based on the proximity to the lower level by direct calculations.

As can be seen, the switching time t will range from zero to 100% of the switching period and is the time that should be spent at the upper level. The final step is scheduling the switching transitions. The pulse is left-justified in the switching period starting at the upper level and transitioning to the lower level.

Usually, the nearest levels and switching times for each phase are calculated in a DSP. This information is then transferred to a PLD which operates at a higher clock frequency and can make the transitions of the switching state on a nanosecond time scale. In a practical implementation, the DSP and PLD clocks are tied together by a PLD circuit which divides its clock and sends a clock signal to the DSP on the microsecond time scale. Besides the zero-order hold effect, there is a one-sample delay effect which is caused by the fact that the DSP will take some time to determine the levels and switching times. The computed duty cycle (indicated by

the discrete points) is used in the switching period causing a lag between the duty cycle and the switching state. This effect is negligible for high switching frequencies.

Some comments are appropriate to show the equivalence between the discrete implementation and the sine-triangle and SVM methods. The switching state would start in the upper level and transition to the lower level at the appropriate time. An identical switching pattern is obtained in the sine-triangle method by using a saw-tooth waveform instead of a triangle waveform. Likewise, moving the pulses to the right side of the switching period (a transition from the lower level to the upper level) would be equivalent to using a reverse saw-tooth waveform. If the pulses are centered within the switching period, then the result is the same as that using a triangle waveform. Since the sine-triangle and discrete methods are both performed on a per-phase basis and in the time domain, their equivalence is easily understood. The equivalence to SVM can be seen by creating a plot of the switching states for all three phases. The sequence can be reversed in the discrete implementation by switching to right justification. There is much more to the equivalence of these methods including adding harmonics to the duty cycles in the sine-triangle method or changing the dwell times in the SVM method.

It can be seen that the discrete method presented herein relies on computation directly from the duty cycles and therefore it is not necessary to define triangle waveforms or voltage vectors. However, sine-triangle modulation is useful in that it can provide a straightforward method of describing multilevel modulation.

(IV) Space vector control

A rather unique voltage-source modulation method called space vector control (SVC) has been recently introduced. Since it is fundamentally different than sine-triangle or SVM, it is

presented in this separate section. The premise of this scheme is that the inverter can be switched to the vector nearest the commanded voltage vector and held there until the next cycle of the DSP. The concept in the vector domain for a multi-level inverter is that, only one quadrant of the vector plot is shown. The nearest vector to the commanded voltages is determined according to the hexagonal regions around each vector. This operation is performed at each sample period of the DSP resulting in a simple modulation method. Since the vector is held for the DSP cycle, there is no need to compute switching times and schedule timing in the PLD.

Although this method is simple to implement, it is most useful on inverters with a relatively high number of voltage vectors. An example is the eleven-level series H bridge inverter with five cells. Another aspect of this control is that the DSP switching period should be small since the voltage is held constant for the entire switching time. Implementation of this scheme on an eleven-level inverter has shown that it can produce a lower THD than the SVM method.

3.2.2 Current-regulated methods

Although this method directly regulates the currents, it relies on an analog implementation which is not practical for higher power levels. These schemes provide a digital implementation, but have lower harmonic performance than the voltage source methods. The tradeoff between discrete implementation and harmonic performance has been an issue for current-regulated controls.

(i) Hysteresis control

The hysteresis current-control concept typically employed in two-level drive systems can be extended to multi-level systems by defining a number of hysteresis bands. The basic operation of the control involves defining n-1 evenly spaced hysteresis bands on each side of the

commanded current. The voltage level is then increased by one each time the measured current departs from the commanded value and crosses a hysteresis band. One important detail of this control is that the voltage level will be at its highest or lowest value when the measured current crosses the lowermost or uppermost hysteresis band respectively. This ensures that the current will regulate about the commanded value. This straightforward extension of two-level current control results in good regulation of the currents and acceptable voltage level switching. Furthermore, the multi-level hysteresis control handles steps changes in commanded current with a response similar to two-level hysteresis control.

The amount of analog circuitry can be reduced by using a single hysteresis band and increasing or decreasing the voltage levels each time the current touches the band. This method is then coupled with timing and a voltage controlled oscillator to drive the current error to zero. An extension to this method uses two hysteresis bands to provide better dynamic performance, but still utilize a small amount of analog circuitry for a large number of voltage levels. The dual hysteresis band approach has been used in the multi-level inverter where the inner band is used to achieve capacitor voltage balancing and the outer band is used for current regulation.

Three-phase inverter for hysteresis Current Control is shown below.

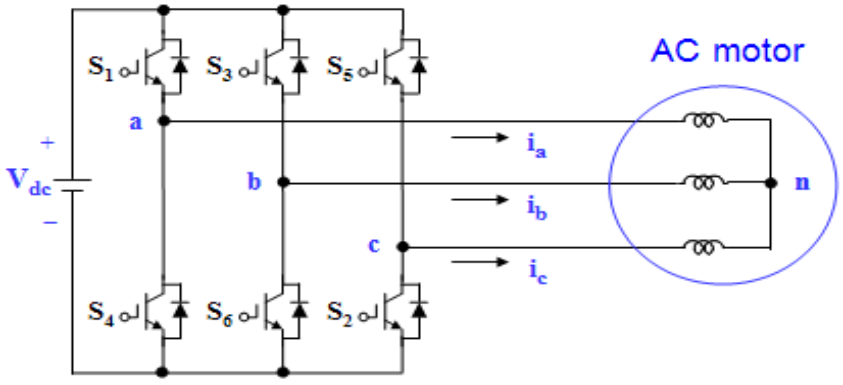

Fig.3.14 Three-phase inverter for hysteresis current control.

Hysteresis Current Controller is shown below.

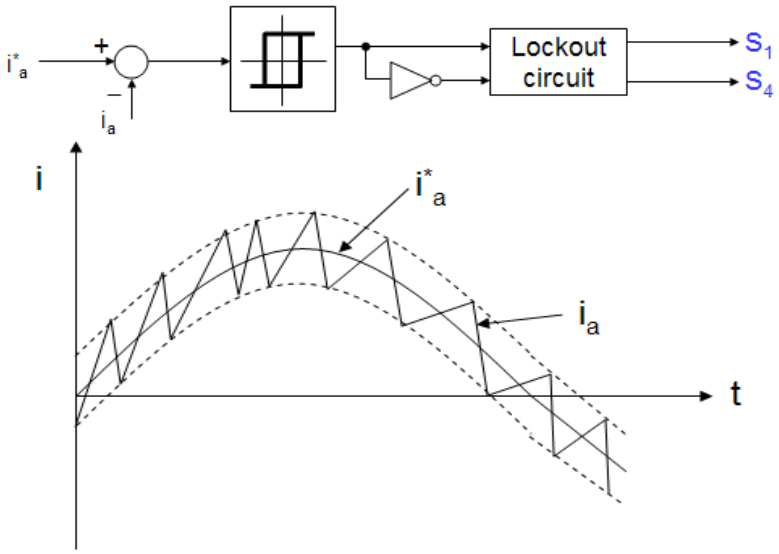

Fig.3.15 Hysteresis current controller at Phase "a".

Characteristics of hysteresis Current Control are discussed below.

Advantages

(i) Excellent dynamic response

(ii) Low cost and easy implementation

Drawbacks

(i) Large current ripple in steady-state

(ii) Variation of switching frequency

(iii) No intercommunication between each hysteresis controller of three phases and hence no strategy to generate zero-voltage vectors. As a result, the switching frequency increases at lower modulation index and the signal will leave the hysteresis band whenever the zero vector is turned on.

(iv) The modulation process generates sub harmonic components.

(ii) Clocked sigma-delta modulation

Some current-regulated schemes are based on the sigma-delta function. Based on the hysteresis level *h*, the per-phase switching state is determined from the current error. The function can be implemented directly with analog components or it can be implemented on a DSP based on a fixed clock frequency. In a two-level system, the hysteresis level is zero and the control reduces to that of standard delta modulation. As with two-level systems, the switching frequency of the inverter may be less than the clock frequency since the voltage level may not change every time the control is clocked. The current tracking improves with increasing clock frequency, and a relatively high frequency is needed for good performance. This makes the control somewhat undesirable, although digital implementation is an advantage.

The concept behind multilevel delta modulation is illustrated here. As with clocked sigma delta modulation, the control operates on a per-phase basis and can be implemented on a DSP. The general scheme functions by increasing or decreasing the voltage level by one at each clock cycle of the DSP depending on whether the current error is positive or negative respectively. In this control, the hysteresis band does not need to be defined.

In the two-level implementation, the control reduces to that of standard delta modulation. As with clocked sigma-delta modulation, the clock frequency must be set relatively high in order to obtain good current tracking.

3.2.3 Common Requirements of PWM Techniques

All low pulse number PWM techniques should observe the synchronism with the fundamental frequency and quarter and half wave symmetry. Synchronism with the fundamental frequency means ensuring the switching frequency fc is an integer multiple of the synthesized fundamental frequency f1. That is, the pulse number $N = fc/f_1$ must be an exact integer. The

frequency spectrum of the PWM waveform will then consist of discrete frequencies at multiples of the fundamental frequency nf_1, where n is an integer.

Quarter and half wave symmetry ensures that no even harmonics will exist in the output spectrum [44]. This can be achieved by choosing N odd. An important even harmonic which is eliminated is the DC component.

No frequency components below the fundamental frequency (commonly referred to as sub-harmonics) will exist. This is important since an undesired harmonic component near zero frequency can cause large currents to flow in inductive loads.

3.3 Carrier Based PWM Techniques. (Fundamental & Carrier waveform relationships)

The carrier frequency is the same as the switch frequency. If the modulation were reduced to zero or a DC quantity, then the PWM spectrum would consist of the carrier and its harmonics alone and the component at zero frequency (DC) if present. As the amplitude of the modulating waveform is increased, sidebands appear and increase in amplitude either side of the carrier and its harmonics. As the frequency of the modulating waveform is increased, the sidebands spread away from the central carrier frequency.

As mentioned, the carrier frequency should be synchronous, that is an integer multiple of the fundamental frequency, if the pulse number is low (say $N < 21$). An odd multiple guarantees half and quarter wave symmetry and therefore no even harmonics in the carrier spectrum.

If the same carrier signal is used to generate all three phase leg PWM signals in a three phase inverter, the carrier spectral terms in the phase leg signals will also be identical (shown in figure-3.16). Thus the carrier spectral terms (but not the carrier sidebands or modulating terms) will be cancelled in the phase to phase waveforms. This is true regardless of the pulse number *N*.

Although the phase relationship between the modulating and carrier waveforms can be arbitrary, it is suggested that the slopes of the triangular carrier and modulating waveform, if sinusoidal in character, should be of the opposite polarity at the coincident zero crossings, especially for low N. This has practical implementation advantages of preserving the accuracy of the edges in analog implementations, and easing the transition between different pulse numbers in systems where this may change during operation. Additionally this 180 degree phase difference (phase relative to the carrier period) results in the minimization of the harmonic losses in an inductive load.

This 180 degree out-of-phase relationship can only exist for odd *N*. Further, the reduction in harmonic losses due to a specific phase relationship between modulating function and carrier is only significant for odd N. To achieve this phase relationship in a three phase inverter for all three phases requires N to be an odd multiple of three (N = 3, 9, 15, 21 . . .), if the same carrier is to be used for all three phases to achieve carrier cancellation in the phase-phase output.

In a multi-level converter with an integer pulse number, only one carrier can ever meet this requirement, as the other carriers are usually phase shifted relative to it. However, if a non-integer synchronous pulse number (that is a mixed fraction such as N = 21/4) is used in a multilevel converter, this phase relationship once again becomes valid.

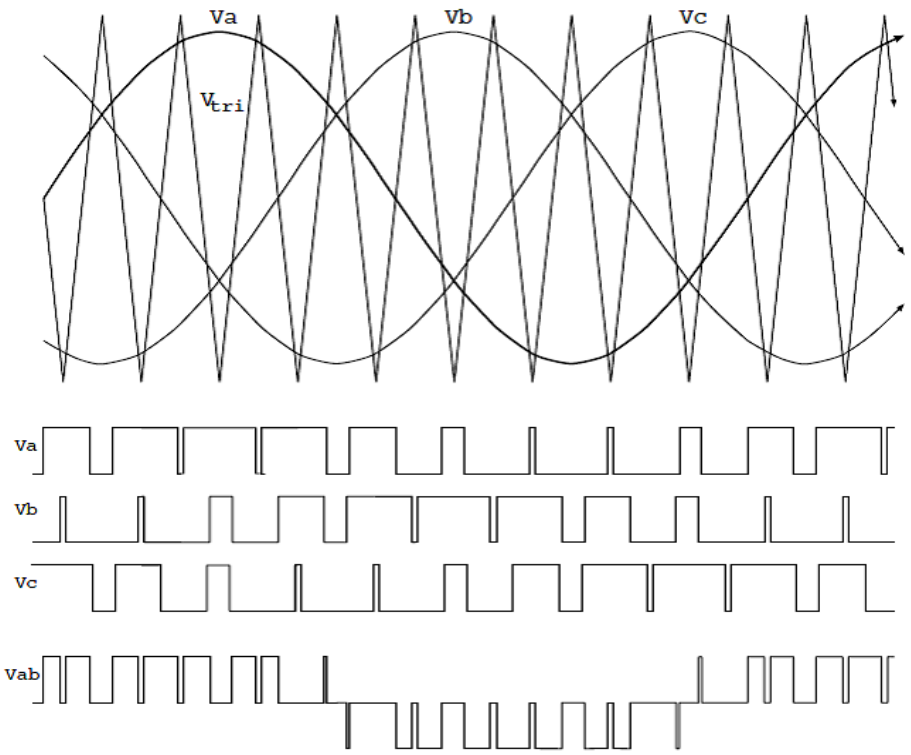

Fig. 3.16: Natural PWM in three phase inverter; phase leg and line to line waveforms.

3.4 Conclusion.

Multi level converters can achieve an effective increase in overall switch frequency through the cancellation of the lowest order switch frequency terms. This chapter has explained different types of carrier based PWM modulation techniques.PWM method are advantageous in controlling the output voltage and reducing the harmonics. There are many modulation techniques for multi level inverters. But carrier based modulation technique is easy and efficient. The PWM output spectra were calculated from basic operation explained above in phase disposition method and simulated using MATLAB (SIMULINK).

Chapter 4

SIMULATION AND RESULTS DISCUSSION

Simulation of Three level Inverter

Simulation of Five level Inverter

Simulation of Seven level Inverter

Experimental setup.

Performance characteristics of induction motor connected to multi level inverter.

4.Simulation

To show the performance of the proposed cascaded converter, an adjustable-speed induction motor drive is studied. The proposed converter synthesizes a three-phase multilevel waveform from the calculated switching angles. The converter thus generates the variable-amplitude, variable frequency voltage waveforms to drive the induction motor. The MATLAB-simulink is used is used to simulate 3, 5 and7- level inverters induction motor drives, where all parameters and blocks are modeled based on basic concepts explained in chapter 2. One of the key features is that it allows the user to simulate the design over a specified period of time. This way it is possible to analyze the time response of control system. For experimental verification FPGA is used as the main controller.

4.1 Simulation of Three-Level Cascade Inverter Induction Motor Drive

Three level inverter is modeled based on the theoretical concepts explained in chapter 2. Here the sub system for pulse generator is modeled where one reference wave (sine wave) and two carrier waves (triangular wave) are taken. First triangular wave is applied across the positive half cycle of the sine wave and second triangular wave is applied across negative half cycle of the sine wave.

Based on the concepts explained in modulation techniques, four pulses are generated. Theses pulses are given to the switches in one phase leg of a three level inverter. Similarly the pulses are generated for remaining two phases, just by changing phase shifting angle of modulating signal by 120 degrees. Fig 4.1 represents the model of a 3-level cascaded inverter. Fig 4.2 represents the carrier modulation signals of the 3-level inverter where one sinusoidal wave is compared with two triangular waves.

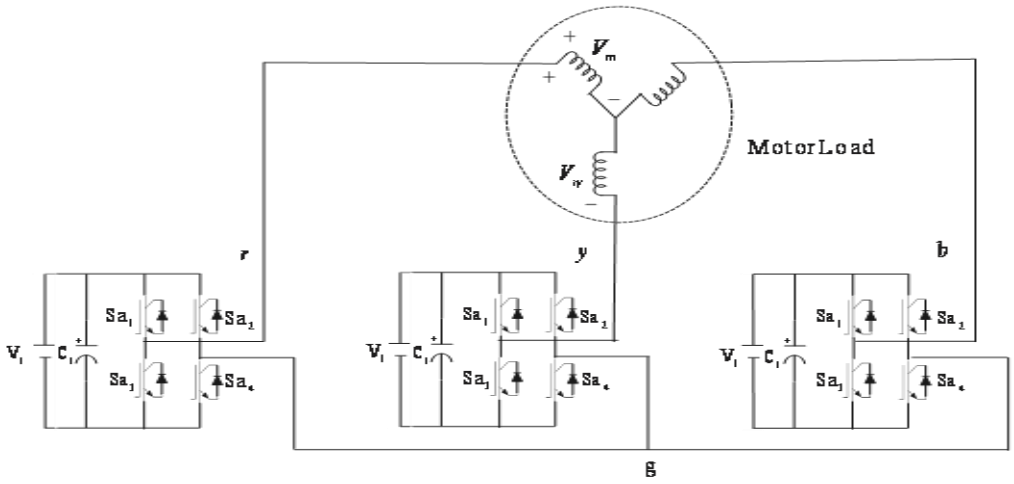

Fig 4.1 Three-level cascaded inverter

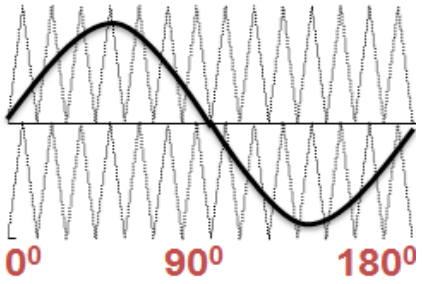

Fig 4.2 Carrier-Modulation Signals of 3-level Inverter.

4.1.1 Simulation Results

Figs. 4.3- 4.10 shows the phase voltage, line voltage, load current, motor speed, torque, stator current , rotor current & THD of a 3-level inverter. Table 4.1 represents THD at different modulation indices. It can be observed that there are very few notches in the voltage and current waveforms. The open-loop speed response of the motor driven by the proposed converter has been shown in Fig.4.6. In steady state, a small-speed ripple is introduced due to the harmonics of the output voltage, specifically the fifth and seventh harmonics. Similarly the torque shown in Fig.4.7 contents some ripples because of harmonics. From Fig. 4.10, which represents the harmonic spectrum, it can be observed that the total harmonic distortion (THD) for the phase

voltage is 39.78% at a modulation index of 1. THD value changes according to the modulation index value which is given in Table-4.1.

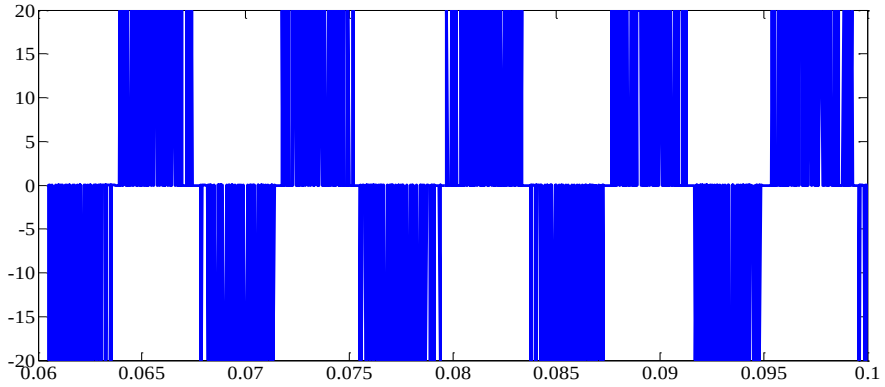

Fig.4.3 Phase voltage Vao of 3-level Inverter.

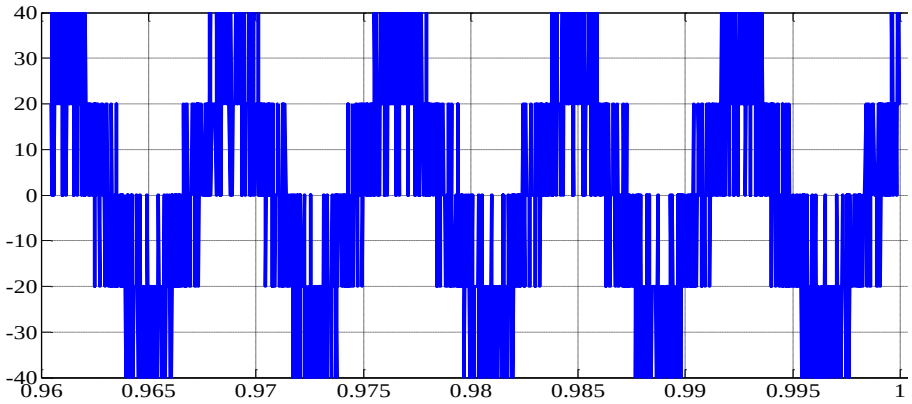

Fig.4.4 Line voltage of 3-level Inverter.

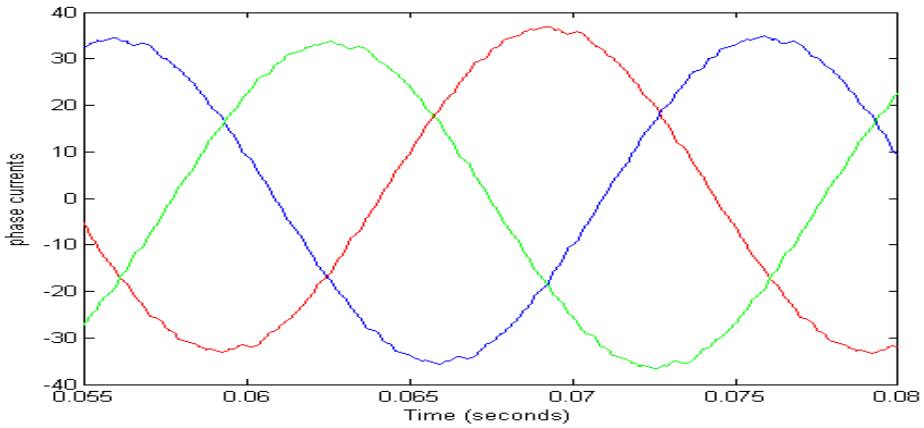

Fig.4.5 Output Currents of 3-level Inverter.

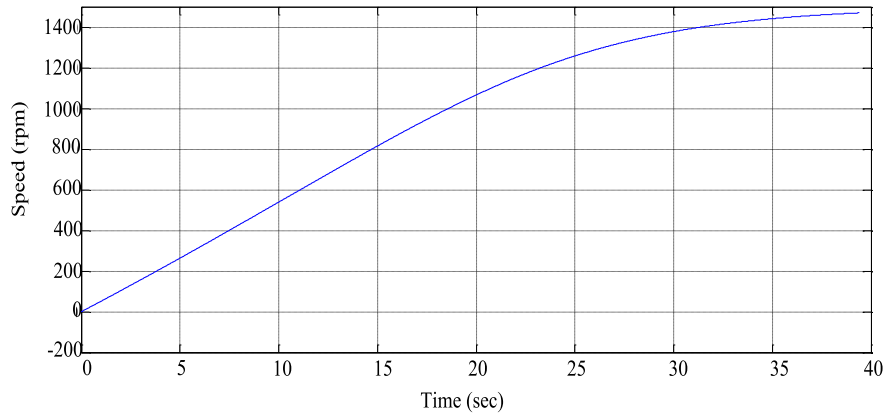

Fig 4.6 Speed of IM in 3-level CMLI.

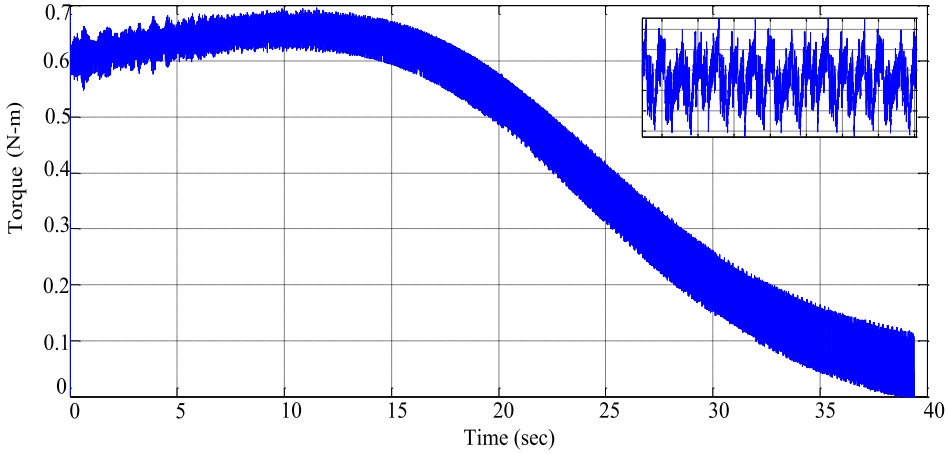

Fig 4.7 Torque of IM in 3-level CMLI.

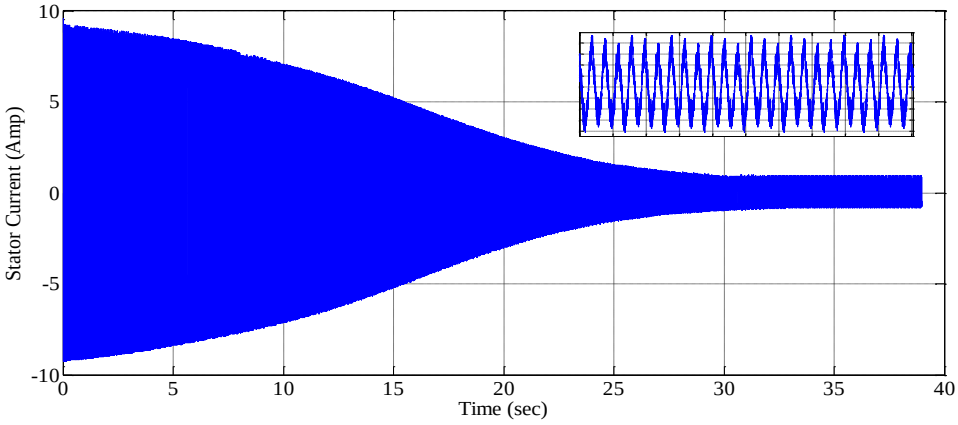

Fig.4.8 Stator Currents of IM in 3-level CMLI.

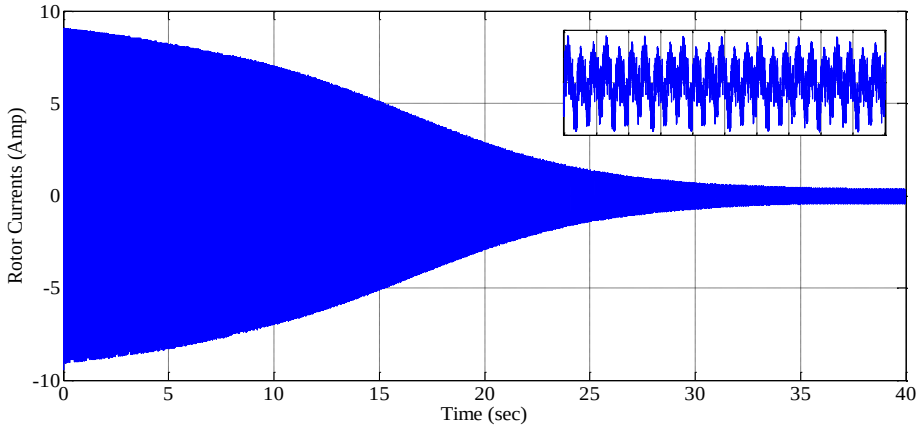

Fig.4.9 Rotor Current of IM in 3-level CMLI.

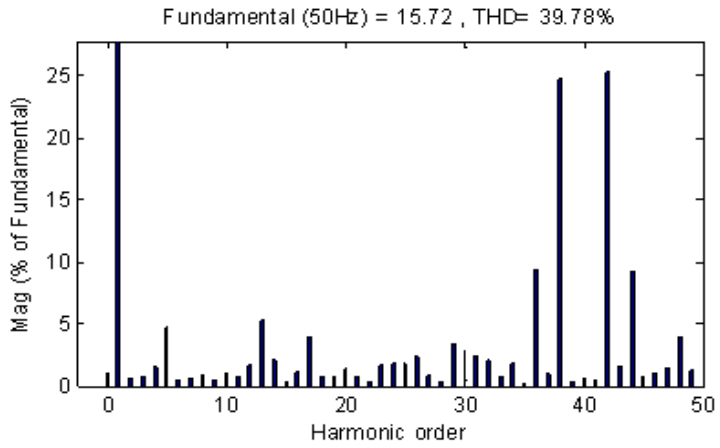

Fig 4.10 Harmonic Spectrum of 3- level Phase Voltage at modulation index=1.

TABLE-4.1 Modulation Index Vs THD in a 3-level Inverter

Modulation Index	THD
1	39.78
0.9	42.69
0.8	45.23
0.7	48.06
0.6	26.39
0.5	30.64
0.4	41.15
0.3	43.31
0.25	50.98

4.2 Simulation of Five Level Cascade Inverter Induction Motor Drive

Five level inverter is modeled in the same way as the three level inverter. The difference here is the number of carrier signals. Here we are taking four carrier signals. Two of them are applied across the positive half cycle of the modulating signal, remaining two of them are applied across the negative half cycle of the modulating signal. From these signals eight PWM signals are generated and then given to the eight switches of a leg. Similarly the pulses are generated for remaining phases. The only difference is that the modulating signal is phase shifted by 120 degrees. Figure 4.11 shows the model of a 5-level cascaded inverter. Figure 4.12 shows the carrier modulation signal of a five-level cascaded inverter.

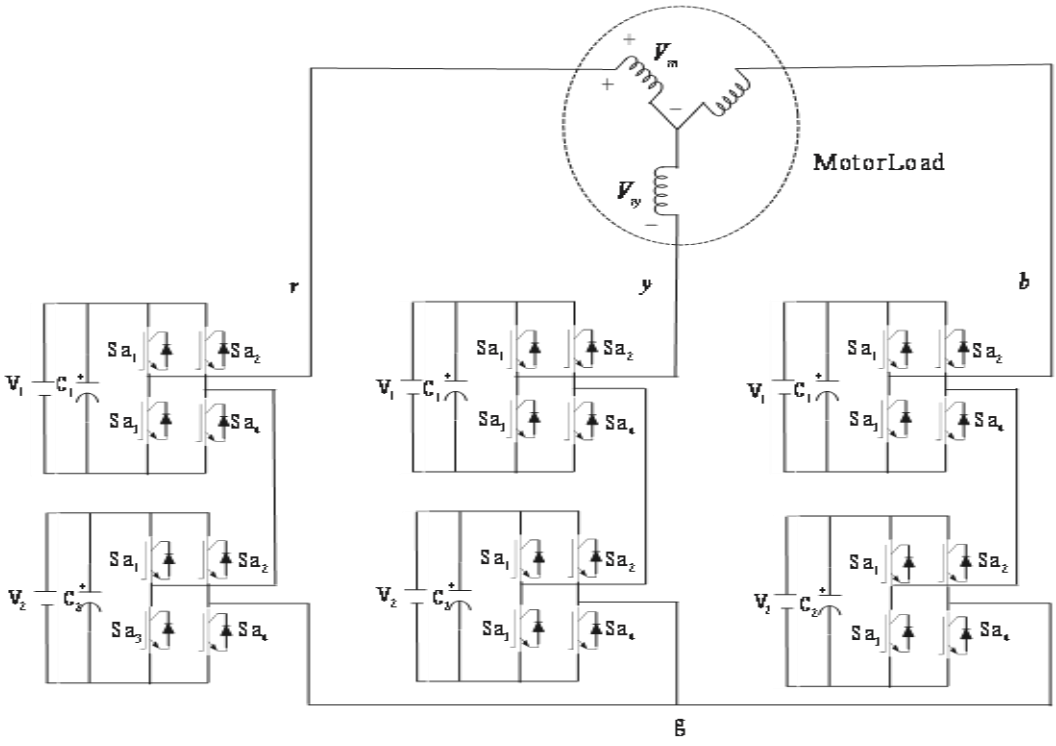

Figure 4.11 Five-level cascaded inverter

4.2.1 Simulation Results

Figs. 4.13- 4.20 shows the phase voltage, line voltage, load current, motor speed, torque, stator current , rotor current & THD of a five-level inverter. Table 4.2 represents THD at different modulation indices. By comparing the three level inverter and the five level inverter we can say that the distortion in five level inverter voltage is less. The current waveforms are closed to sinusoidal. The speed and torque ripples are very less as compared to three level inverter. Dynamic response is also better for five level inverter, which can be observed from the speed and torque waveforms. Fig 4.20 represents the harmonic spectrum analysis of a five level inverter. In this case, the Total Harmonic Distortion is 33.02% for modulation Index 1.The THD for different modulations are given in Table-4.2.

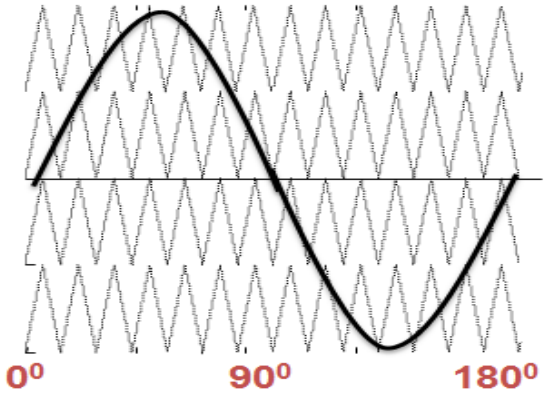

Fig 4.12 Carrier-Modulation signals for five level Inverter.

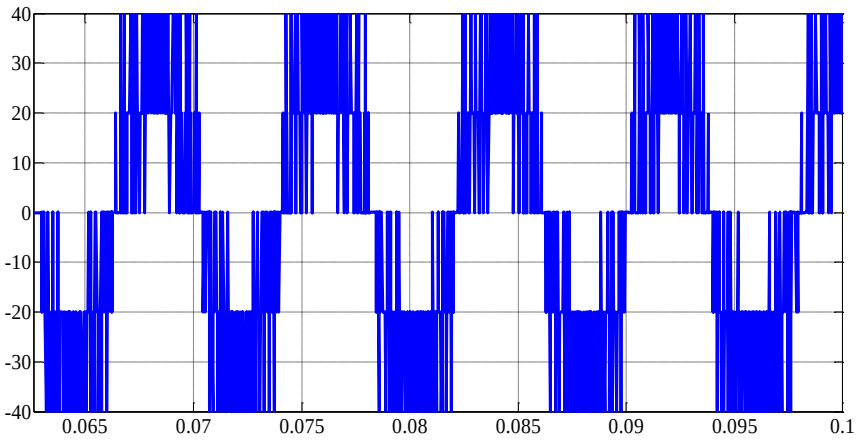

Fig 4.13 Phase Voltage of a five-level inverter.

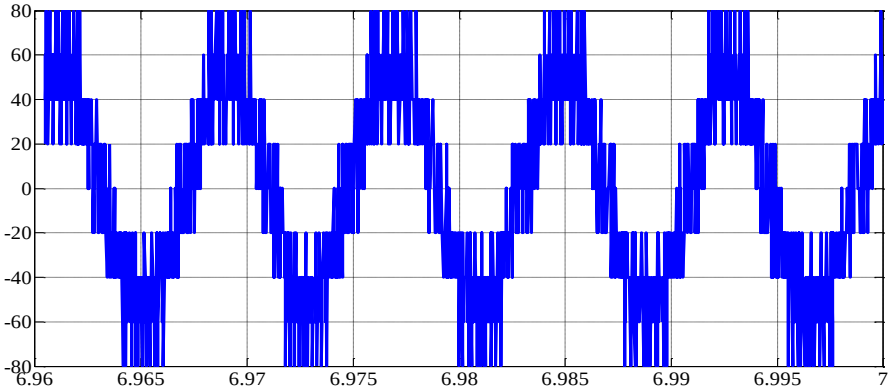

Fig 4.14 Line Voltage of 5-level inverter.

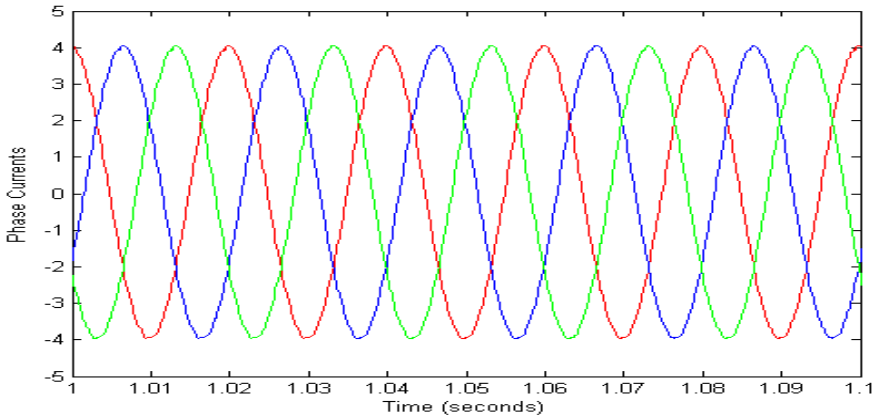

Fig 4.15 Output Currents of 5-level inverter.

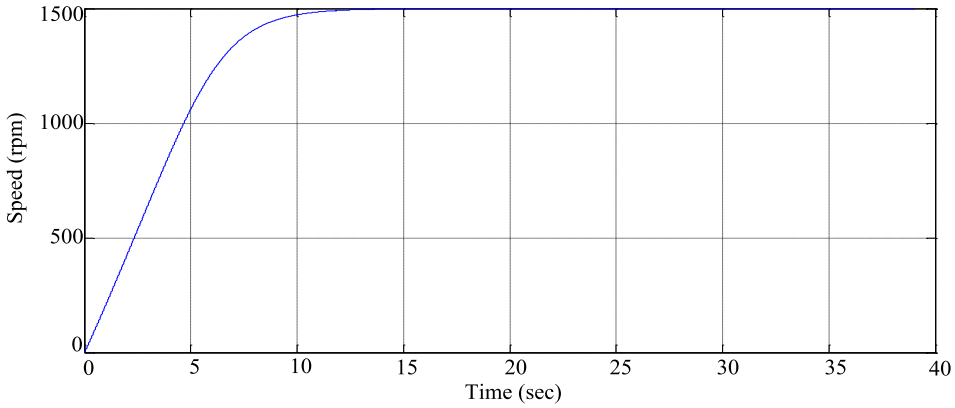

Fig 4.16 Speed of IM in 5-level CMLI

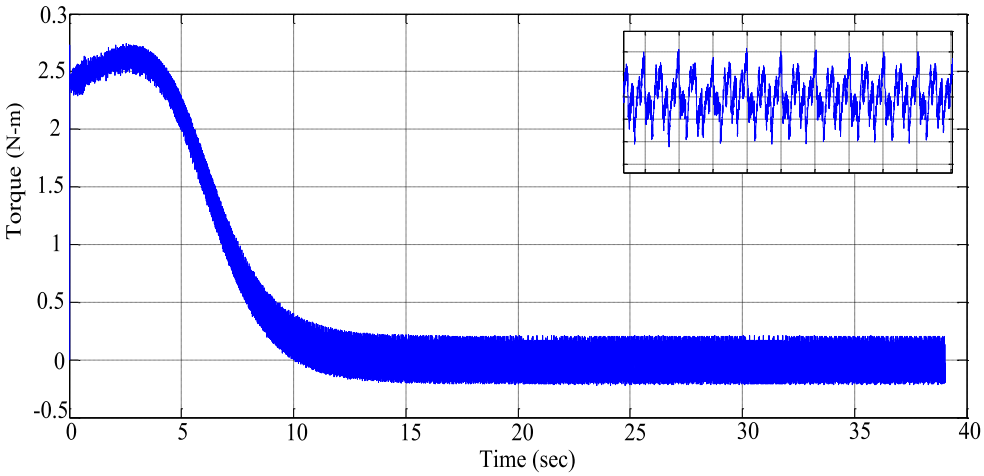

Fig 4.17 Torque of IM in 5-level CMLI. .

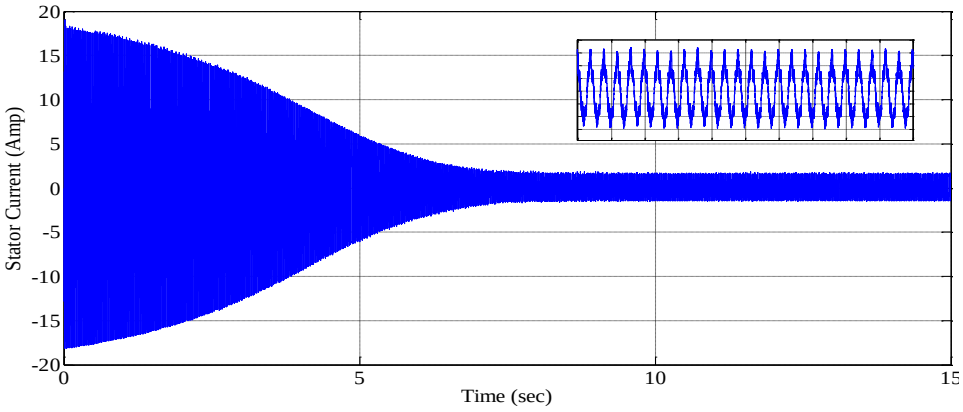

Fig 4.18 Stator Currents of IM in 5-level CMLI.

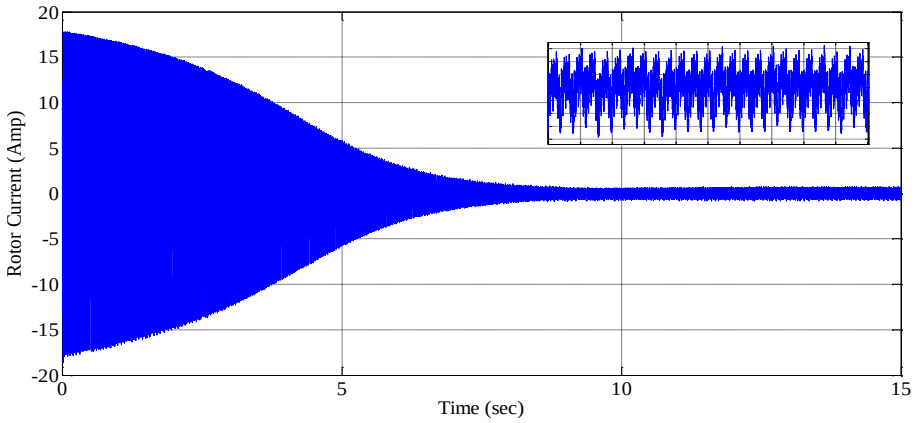

Fig 4.19 Rotor Current of IM in 5-level CMLI.

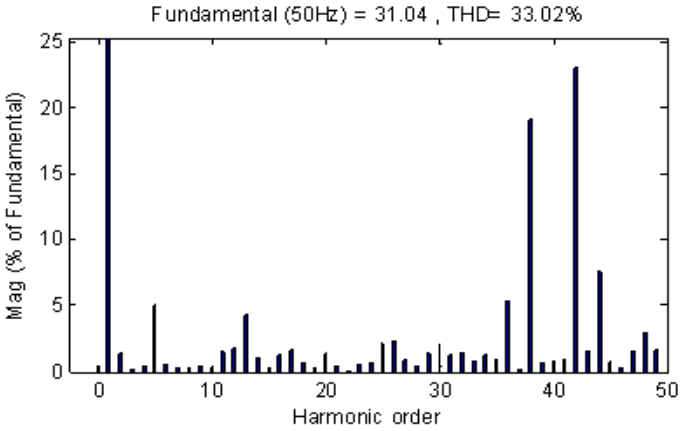

Fig 4.20 Harmonic Spectrum of Five level Inverter Phase Voltage at modulation Index=1.

Table-4.2 Modulation Index Vs THD in a 5-Level Cascaded Inverter

Modulation Index	THD
1	33.02
0.9	33.51
0.8	35.50
0.7	38.22
0.6	20.61
0.5	24.62
0.4	34.06
0.3	36.03
0.25	40.49

4.3 Simulation of Seven Level Cascade Inverter Induction Motor Drive

Seven level inverter is modeled similar to that of the three-level and five-level inverter. The difference here is also the number of carrier signals. Here we are taking six carrier signals. Three of them are applied across the positive half cycle of the modulating signal. Remaining three of them are applied across the negative half cycle of the modulating signal. From these signals twelve PWM signals are generated and then given to the eight switches of a leg. Similarly the pulses are generated for next two phases. The only difference is that the modulating signal is phase shifted by 120 degrees. Fig 4.21 shows the model of a 7-level cascaded inverter. Fig.4.22 shows the carrier modulation signal of a seven-level cascaded inverter.

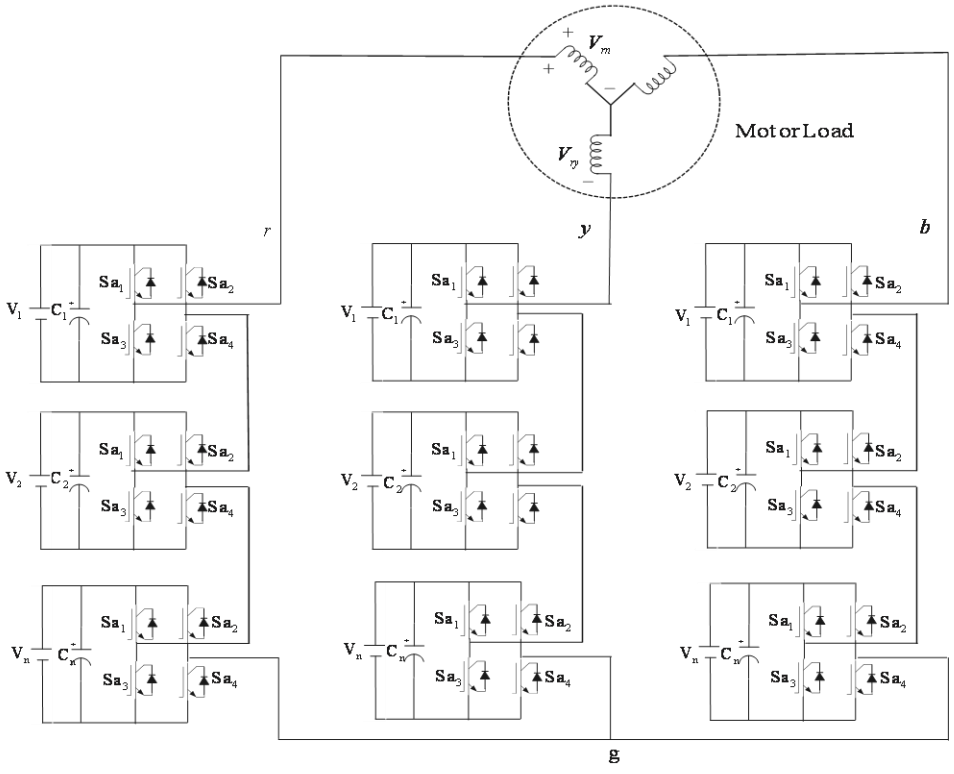

Fig 4.21 Model of a Seven-level cascaded inverter.

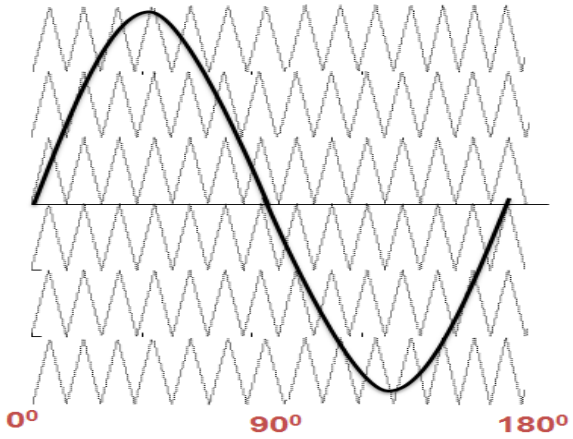

Fig.4.22 Carrier-Modulation signals for seven level Inverter.

4.3.1 Simulation Results

Figs. 4.23- 4.29 shows the phase voltage, line voltage, motor speed, torque, stator current , rotor current & THD of a seven level inverter. Table 4.3 represents THD at different modulation indices. By comparison we can say that the distortion in seven level inverter voltage is less. The current waveforms are much closer to sinusoidal. The speed and torque ripples are very less as compared to three-level and five level inverters. The dynamic response is much better than three and five level inverters. Fig 4.29 represents the harmonic spectrum analysis of a seven level inverter. In this case, the Total Harmonic Distortion is 21.36% for modulation Index 1.The THD for different modulations are given in Table-4.3.

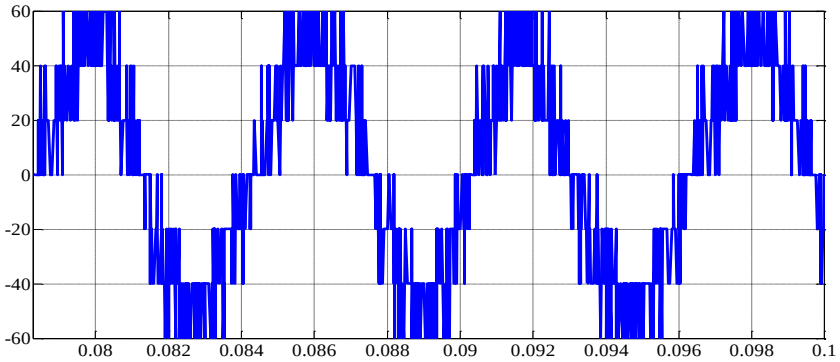

Fig 4.23 Phase Voltage of a 7-level cascaded inverter.

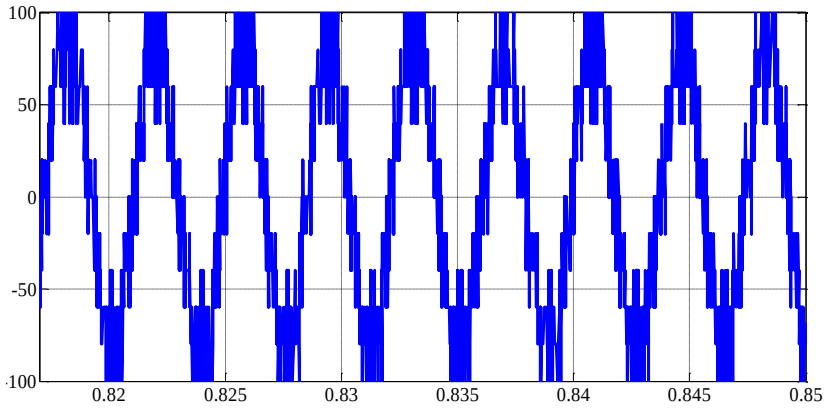

Fig.4.24 Line voltage of 7-level cascaded inverter.

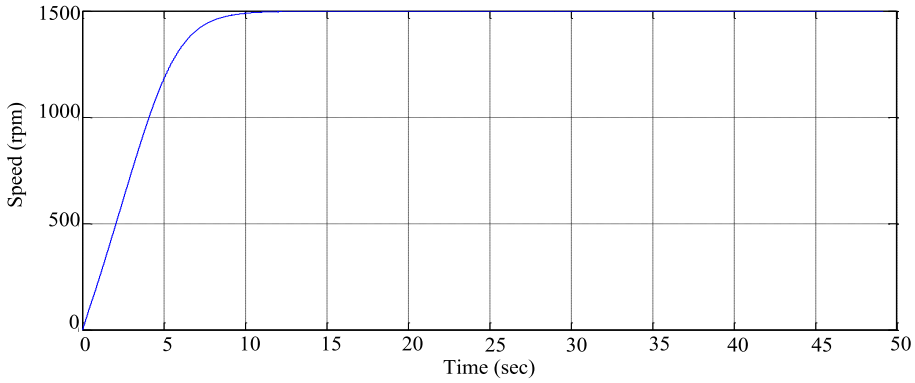

Fig 4.25 Speed of 7-level cascaded inverter

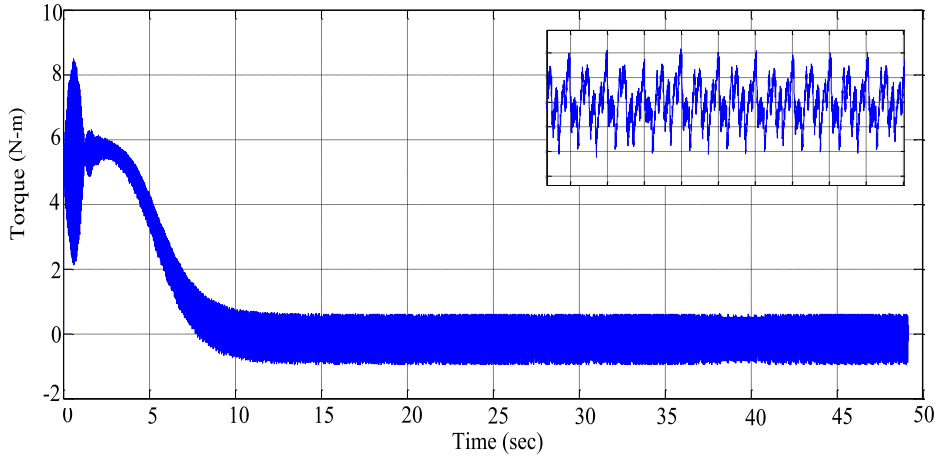

Fig 4.26 Torque of 7-level cascaded inverter.

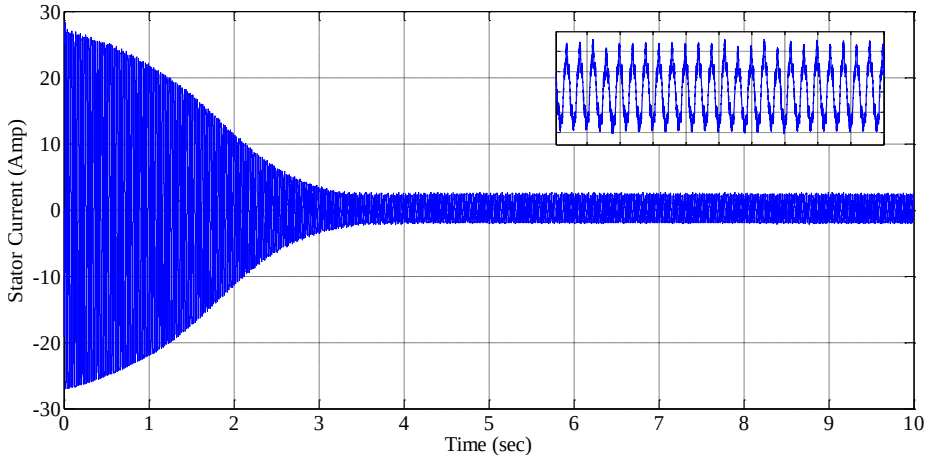

Fig 4.27 Stator current of 7-level cascaded inverter.

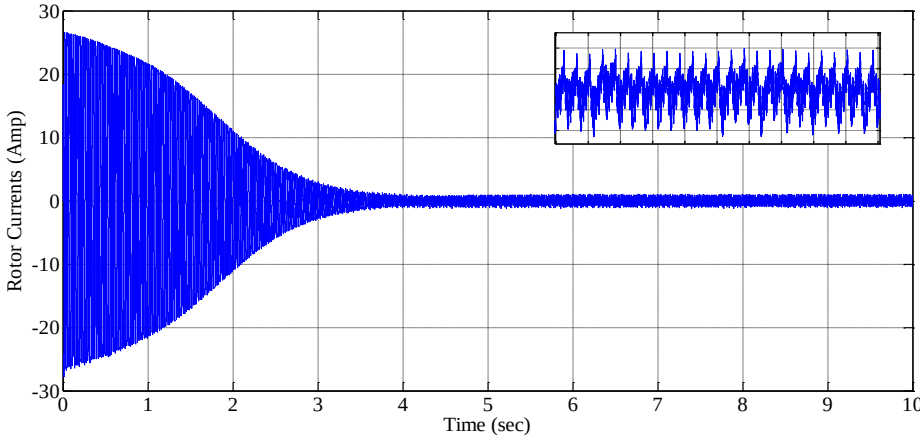

Fig 4.28 Rotor current of 7-level cascaded inverter.

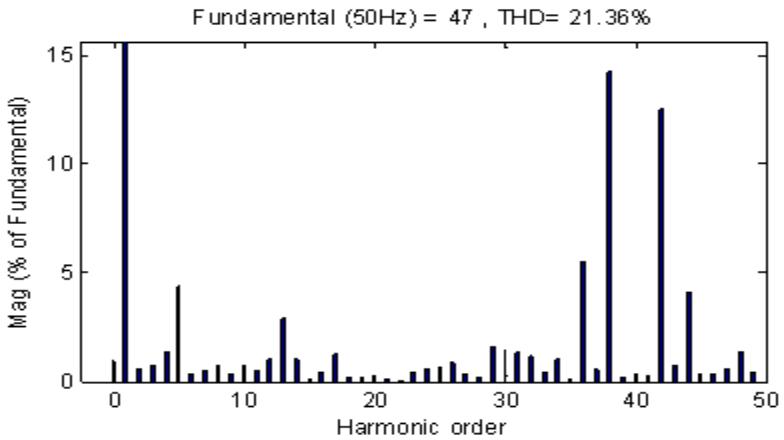

Fig 4.29 Harmonic Spectrum of 7- level Inverter Phase Voltage at modulation Index=1.

Table-4.3 Modulation Index Vs THD in a 7-Level Inverter

Modulation Index	THD
1	21.36
0.9	23.28
0.8	24.79
0.7	25.79
0.6	15.15
0.5	20.06
0.4	28.36
0.3	29.47
0.25	31.27

4.4 Comparison

The comparison between the total harmonic distortion with respect to the modulation index for 3, 5 and 7-level cascaded inverter is shown below in figure 4.30. It can be observed that the THD is better in 7- level inverter.

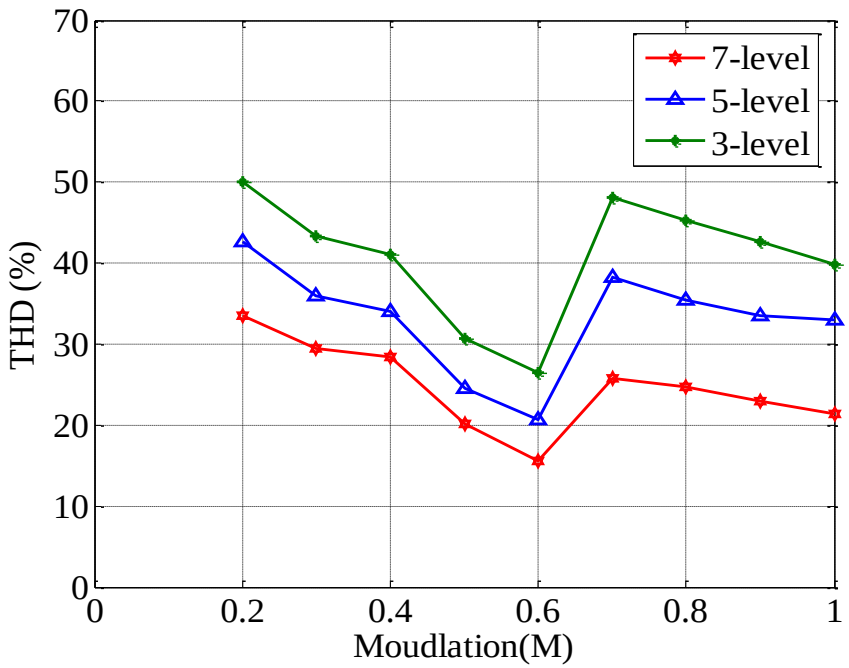

Fig. 4.30 THD vs MI of 3,5 and 7-level Inverter

4.5. Experimental setup

To verify the simulation results, a multilevel voltage source converter (VSC), which can be used for 3-level, 5-level & 7level, using cascaded converters with separated DC sources, as shown in Fig.4.32 is used as a hardware prototype. Nine IGBT modules are used as the main switches, which are connected in full-bridge converter configuration. Each power stage is supplied by a variable DC source. Here the PWM signal is generated through FPGA.In the control circuit, two FPGA from Xilinx Spartan3 device XC3S400-4PQ208 are employed to generate the necessary gate drive signals. The different parameters of the IM are given below.

Voltage = 415 v (±10%), Power = 750 watt

Current = 1.8 amp. Frequency = 50 Hz (±5%)

Power Factor = 0.8, Speed = 1415 rpm

Fig 4.31. Experimental setup for cascaded multilevel inverter

4.5.1 Experimental Result

Figs. 4.32 – 4.34 shows the experimental results of phase voltages, load currents of 3, 5 and 7-level cascaded inverter respectively. The THD at modulation index 1 for 3, 5 and 7-level cascaded inverter are shown in fig 4.35-4.37.

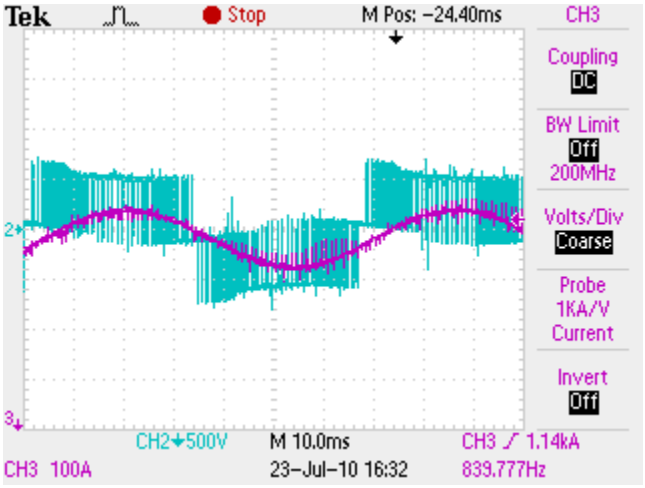

Fig 4.32 Output voltage and current of 3-level cascaded inverter

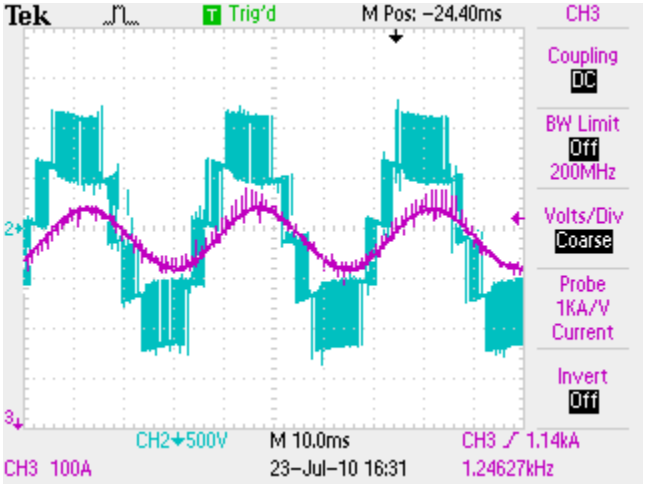

Fig 4.33 Output voltage and current of 5-level cascaded inverter

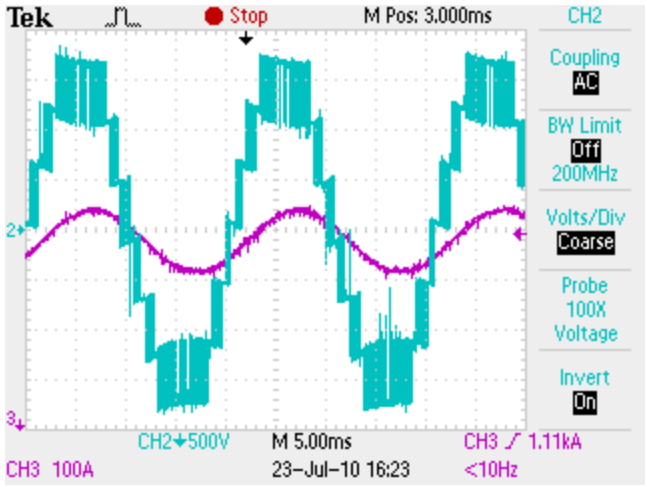

Fig 4.34 Output voltage and current waveform of 7-level cascaded inverter

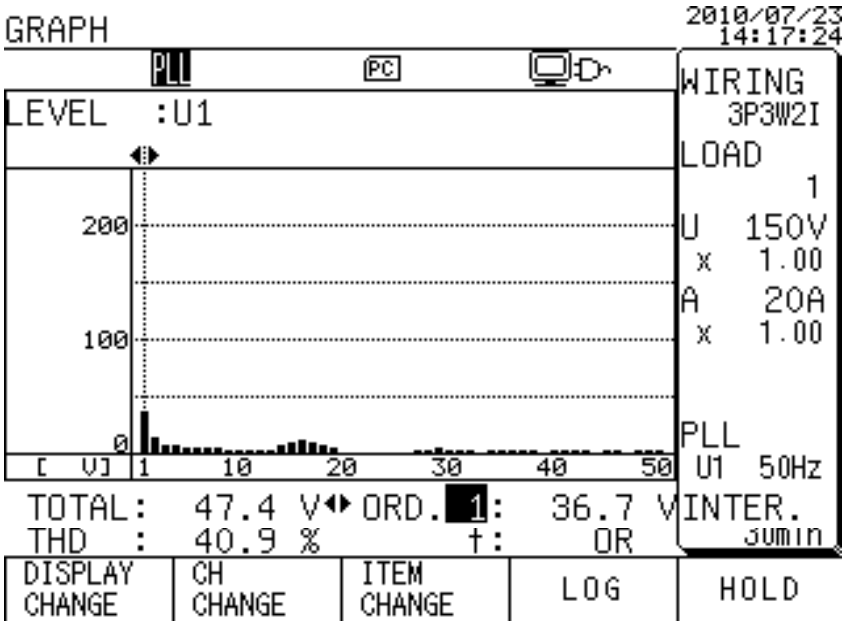

Fig 4.35 THD of 3-level cascaded inverter.

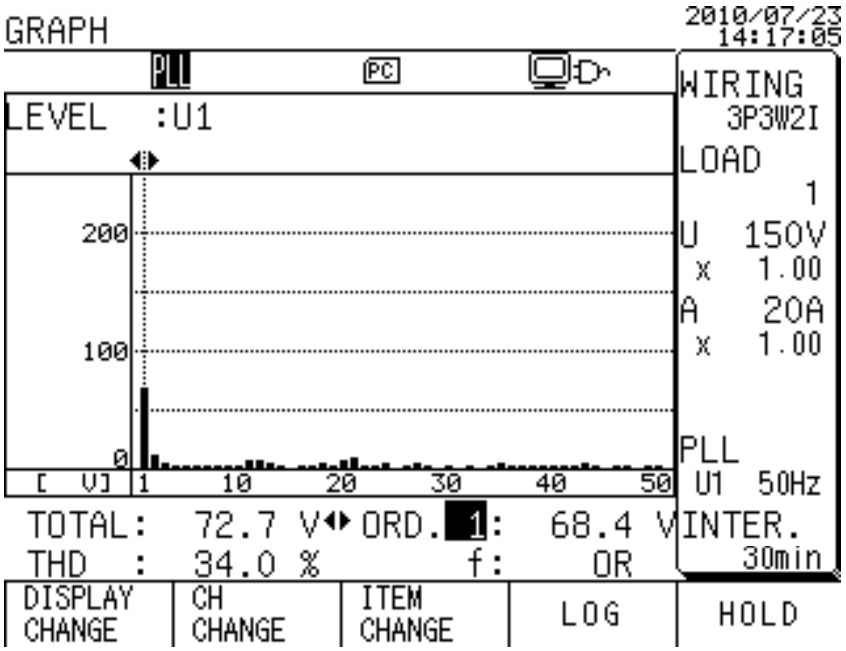

Fig 4.36 THD of 5-level cascaded inverter

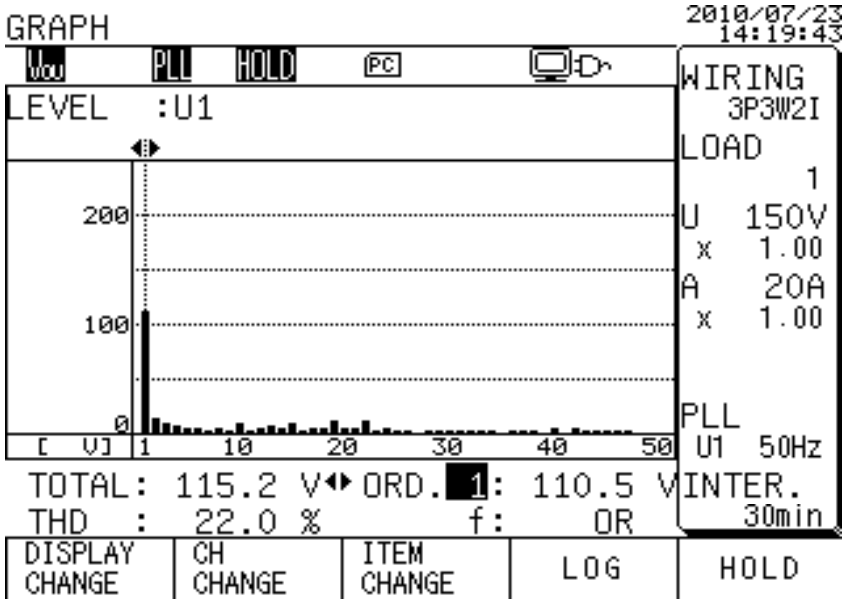

Fig 4.37 THD of 7-level cascaded inverter

4.5.2 Conclusion

This chapter presented the performance of multilevel inverter induction motor drives. The simulation and experimental results are in close agreement. We can observe that the quality of voltage and current waveforms increases with voltage level. The notches in the current and voltage waveforms reduce with increase in voltage level. Thus comparing the results it is observed that harmonic content has been predominantly reduced and drives performance improved.

Chapter 5

CONCLUSION & FUTURE WORK

Conclusion

Future Work

5.1. Conclusion.

This thesis has provided a brief summary of multilevel inverter circuit topologies (3-level, 5-level and 7-level) and their analysis with respect to induction motor drives.

Each MLI has its own mixture of advantages and disadvantages and for any one particular application, one topology will be more appropriate than the others. Often, topologies are chosen based on what has gone before, even if that topology may not be the best choice for the application. The advantages of the body of research and familiarity within the engineering community may outweigh other technical disadvantages. Multilevel converters can achieve an effective increase in overall switch frequency through the cancellation of the lowest order switch frequency terms. As discussed in Chapter 2, among the multilevel converter topologies, the CMC is the most promising alternative for industry application.

In the third chapter, we have discussed different types of carrier based PWM modulation techniques. There are many modulation techniques for multi level inverters. But carrier based modulation technique is easy and efficient. The PWM output spectra were calculated from basic operation simulated using MATLAB.

The simulation results for three-level, five-level and seven-level cascaded inverters are presented in chapter-4. Their harmonic analysis is also discussed. THD of the three cascaded multi-level inverters have been calculated at different modulation index. Their speed and torque are compared. We have observed that the performance of the induction motor drive improves with increase in voltage level of the inverter. The simulation results show that the CMC Induction Motor drives has a satisfactory performance. To verify the simulation results, a CMC, using separated DC sources is used as a hardware prototype. Both simulation and experimental results are in close agreement.

Today, worldwide research and development of multilevel inverter-related technologies are going on. The focus of this thesis is limited to fundamental principle of different multilevel inverters, modulation technique, and harmonic analysis of induction motor drives.

5.2 Future Work

Although this dissertation has covered most of the interesting issues and challenges of the Cascaded multi-level inverter induction motor drives, additional work has been left for future research.

The first part is the fault-protection study for the cascaded multi-level inverter induction motor drives. Due to the excessive number of semiconductor devices and passive components, how to design a fault protection scheme to enhance the ride-though capability in various fault scenarios remains as an important challenge. In industrial applications, the faulty module is to be replaced, while the converter is running. Therefore an additional switch is required at the terminal points of the module connections. Experimental tests have shown that when such an error occurs, the voltage is equally distributed among the remaining modules, such that it matches the DC-link voltage, as before. In this way the stability of the system under module fault conditions is ensured. Further investigation is to be made in this field as well.

The second part is the redundancy of the cascaded multi-level inverter induction motor drives. Due to the identical HBBBs used in the CMC, the N+1 rule may be applied, where N is the number of HBBBs per phase. The seven-level cascaded converter, for example, can have four HBBBs instead of three. In case of a semiconductor failure in one HBBB in the same phase leg, the rest of the HBBBs can still generate a normal output voltage.

The next step in the three-phase experimentation procedure is testing the converter on an induction motor drive using conventional torque and speed control structures. Decisions on the switching frequency and the capacitor dimensioning are to be reached and the implementation software still is to be built.

Since one of the assets of the specific converter is that it can operate in low switching frequencies, a comparative study of the power losses is interesting to be carried out for high-power applications, including switching and conducting losses.

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